

# Performance Communications Appliance for the Intel(R) Pentium(R) M Processor

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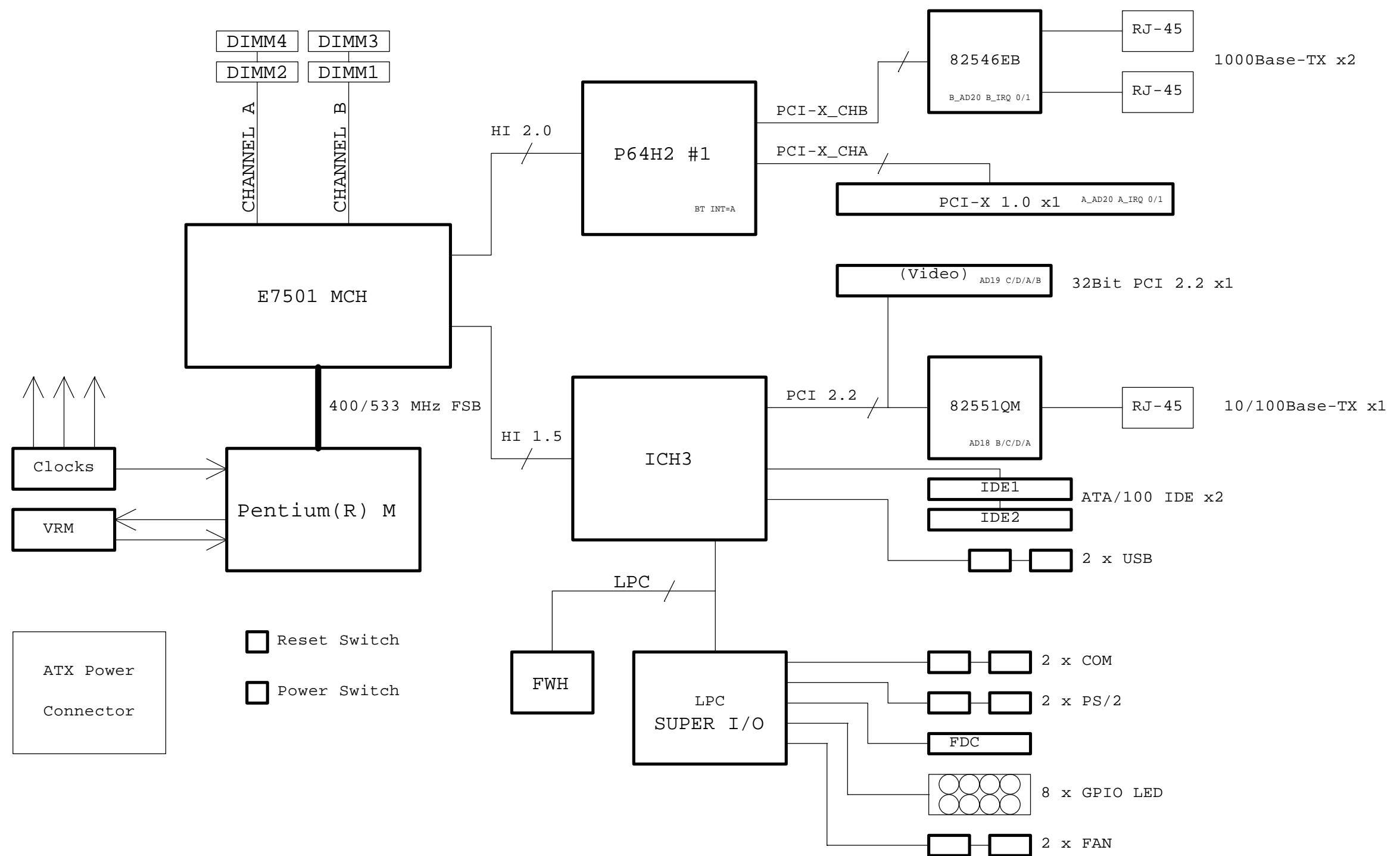
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Initial Release: REV. A0

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# Performance Communications Appliance for the Intel(R) Pentium(R) M Processor

## Block Diagram



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1.Route pin AE7,AF6 VCCSENCE,VSSSENSE differential

CPU Strapping: CPU\_TEST[3..1],CPU\_TDI,CPU\_TMS,CPU\_TRST#,CPU\_TCK  
Route 5:10, L=2.0"

2.Route following common clock signals 4:8, 3.0" < L <6.5"  
No TLM(trace length match) requirement. but route on same layer  
HADS#, HBNR#, HBPM#[5..0], HBPRI#, P0\_BREQ#0,  
HDRDY#, HDBSY#, HDEFER#, DDPWR#, HTRDY#,  
HIT#, HITM#, HLOCK#, HRS#[2..0], HCPURST#

3. Source Synchronous Signal List

signals	matching	relative to
HREQ#[4..0], HA#[16..3]	+/-200mil]	HADSTB#0
HA#[31..17]	+/-200mil]	HADSTB#1
HD#[15..0], HDBI#0	+/-100mil	HDSTBP#0, HDSTBN#0
HD#[31..16], HDBI#1	+/-100mil	HDSTBP#1, HDSTBN#1
HD#[47..32], HDBI#2	+/-100mil	HDSTBP#2, HDSTBN#2
HD#[63..48], HDBI#3	+/-100mil	HDSTBP#3, HDSTBN#3

Signals within its associated strobe group must be route on the same internal layer for the entire length of the bus and reference to ground.  
Strobes: 5:15, 3.0"<L<7.5"  
HDSTBP#[3..0], HDSTBN#[3..0], HADSTB#[0..1]  
TLM of +/-25mil to +/- strobe pair

4. Asynchronous signals:  
A20M#, ICH3\_DPSP#L#, FERR#, IERR#, IGNNE#  
INIT#, LINT0\_INTR, LINT1\_NMI, PROCHOT#, CPUPWRGD  
CPU\_SMI#, CPU\_SLP#, STPCLK, THERMTRIP#

5. Hub link interface

a. PSTRBSA,PSTRBFA,PSTRBFA,HIA[0..11],PSTRBFB,PSTRBSB,PSTRBFB,HIB[0..18]  
Route 5:15 3.0" < L < 20.0"

b. HIRCOMPB,HIVSWINGB,HIVSWINGA,HIVREFA must be less than 3.5" from divider to pin

c. HIRCOMPB,HIRCOMPA,less than 1.0"

d. less the 4 vias per signal

e. Keep all strobe/data group on same layer

6. DDR interface

a. DDRA\_DRCOMP, DDRB\_DRCOMP less than 1.0"

b. DDRACLK0,DDRA\_CLK0#,DDRA\_CLK1,DDRB\_CLK0,DDRB\_CLK0#,DDRB\_CLK1,DDRB\_CLK1#,  
route 7.5 : 20

c. DDRA\_CLK0/DDRA\_CLK#0 to DIMM1= 4.0" +/-250mil  
DDRA\_CLK1/DDRCLK#1 to DIMM1 = 6.0" +/-250mil  
DDRCLK0/DDRCLK#0 to DIMM1= 4" +/-250mil  
DDRCLK0/DDRCLK#0 to DIMM1= 6" +/-250mil  
DDRA\_CLK0/#0 +/- 2mil, DDRA\_CLK1/#1 +/-2mil  
DDRCLK0/#0 +/- 2mil, DDRCLK1/#1 +/-2mil

DDR Source Clocked signals  
DDRA\_MA[12..0],DDRA\_CASR#,DDRA\_RASR#, DDRA\_WER#, DDRA\_BAR[0..1]  
DDRCLK\_MA[12..0],DDRCLK\_CASR#,DDRCLK\_RASR#,DDRCLK\_WER#,DDRCLK\_BAR[0..1]  
a.Route 5:15, 2.0"< L <6.0" to DIMM1 for channel A  
b.Route 5:15, 2.0"< L <6.0" to DIMM3 for channel B  
c.Last DIMM to RTT less than 0.8"

DDR Source Synchronous Signals:  
DDRA\_DQ[63..0]+DDRA\_DQR[63..0],DDRCLK\_DQ[63..0]+DDRCLK\_DQR[63..0],  
DDRA\_DQS[17..10]+DDRA\_DQSR[17..10],DDRCLK\_DQS[17..10]+DDRCLK\_DQSR[17..10],  
DDRCLK\_CB[7..0]+DDRCLK\_CBR[7..0]  
a.Route 5 : 15, 0.1" < RS to DIMM1 or DIMM3 < 0.8"  
b.1.8" < MCH to DIMM1 or DIMM3 < 5.5"  
c.Last DIMM to RTT < 0.8"  
d.DQ TO DQS +/- 25mil

DDR Chip Select  
DDRA\_CS#[3..0], DDRCLK\_CS#[3..0]  
a.Route 5:15, L = 4.0" +/-875mil to first DIMM  
b.L = 6.0" +/-875mil to 2th DIMM  
c.0.3" < Last DIMM to RTT < 1.5"

DDR CKE  
DDRA\_CKE0, DDRCLK\_CKE0  
a.Route 7.5:15,  
b.1.8" < L < 6.0"  
c.Last DIMM to RTT

DDR Receive Enable  
DDRA\_RCVENOUT,DDRCLK\_RCVENOUT  
a.Route 5:15  
b.No length match requirement

DDR DRCOMP  
DDRA\_DRCOMP,DDRCLK\_DRCOMP  
a.Route 5:15  
b.L<1.0"

ODTCOMP, MCH\_DDRVREF  
Route 5:10

DDRCVO  
DDRCLK\_CVOH,DDRA\_CVOH  
a.Route 15:20  
b.L < 1.0" from divider

DDR DIMMs Topology

7.ICH3 Hob Interface

a. ICH3\_HITERM,ICH3\_HIREF,must be less than 3.5" from divider to pin

b. ICH3\_HICOMP less than 1.0"

c. less than 4 vias per signals

d. Keep all strobe/data group on same layer

IDE interface

Primary:PDD[15..0],PDA[2..0],PDCS#1,PDCS#3,PDIOW#,PDIOR#,PIORDY,PDDACK#,PDDREQ

Secondary:SDD[15..0],SDA[2..0],SDCS#1,SDCS#3,SDIOW#,SDIOR#,SIORDY, SDDACK#,PDDREQ

a.all IDE route 5:7, length less than 8.0"

b.all IDE length match within +/-250

USB interface

USBP0P, USBP0N, L\_USBP0P, L\_USBP0NUSBP1P, USBP1NL\_USBP1P, L\_USBP1P

a. route differential 5:6, space to other signals and other USB,

b. differential pair 20mil, space to clocks & PCI signals 50mil.

c. Ground reference & as short as possible & minimum vias

d. far away from high speed clocks & signals and avoid parallel.

e. stub length < 200mil,

f. avoid switch layer

g. do not across anti-etch

g. trace length match ;075mil, ICH3 to USB connector

8. Giga Lan i82546EB

a. MDIA0+/- + L1\_A+/- less than 4.0"

b. All differential pair should TLM (+/-25mil)

c. Space between unlike differential pair > 50mil

9. P64H2 clocks

P1A\_PCLK0

a. L1=P1A\_PCLK0 < 1.0"

b. L2=P1A\_PCLKI- 2.5" ;025mil

c. Route 5:15

P1B\_PCLK0

a. L1=P1B\_PCLK0 < 1.0"

b. L2=P1B\_PCLKI ;025mil

c. Route 5:15 Spacing to Other Traces:25mil

10. CLOCKS

BCLK0/BCLK1, HCLKINP/HCLKINN, ITPBCLK0/ITPBCLK1

a. trace width: 5mil

b. Differential pair spacing: 20~25mil

c. Spacing to other trace: 25mil

d. Serpentine Spacing: 5:26

e. Processor to MCH Length Matching:-400mil

f. Differential length matching: +/-25mil

g. Avoid toswitch if possible

CLK66

Trace length L1(RMCH\_CLK66): 0.00 ~ 0.50"

Trace Length L2 (MCH\_CLK66): 3.0" ~ 9.0"

Clock Driver to MCH (RMCH\_CLK66+MCH\_CLK66):L1 + L2 = 3.0 ~ 9.5"= T

Clock Driver to MCH (RICH3\_CLK66+ICH3\_CLK66)=RMCH\_CLK66+MCH\_CLK66=T

Clock Driver to P64H2=T - 0.34"

33MHz PCI Clocks

Trace Length L1:RICH3\_PCLK,RFWH\_PCLK,RSIO\_PCLK,RLAN1\_PCLK

Trace Length L2:ICH3\_PCLK,FWH\_PCLK,SIO\_PCLK,LAN1\_PCLK:0 ~ 0.5"=x1

Trace Length to PCI slot:RP32CLK+P32CLK=X1+X2-2.5": 3.0" ~9.0"=x2

Skew requirement: must be matched to +/-100mil of ICH3\_CLK66

CLK14.318

RICH3\_CLK14 : 0~0.5"

ICH3\_CLK14 : 3.0"~9.0"

Route 5:10

USB Clock

RICH3\_CLK48 : 0~0.5"

ICH3\_CLK48 : 3.0"~12.0"

Route 5:25

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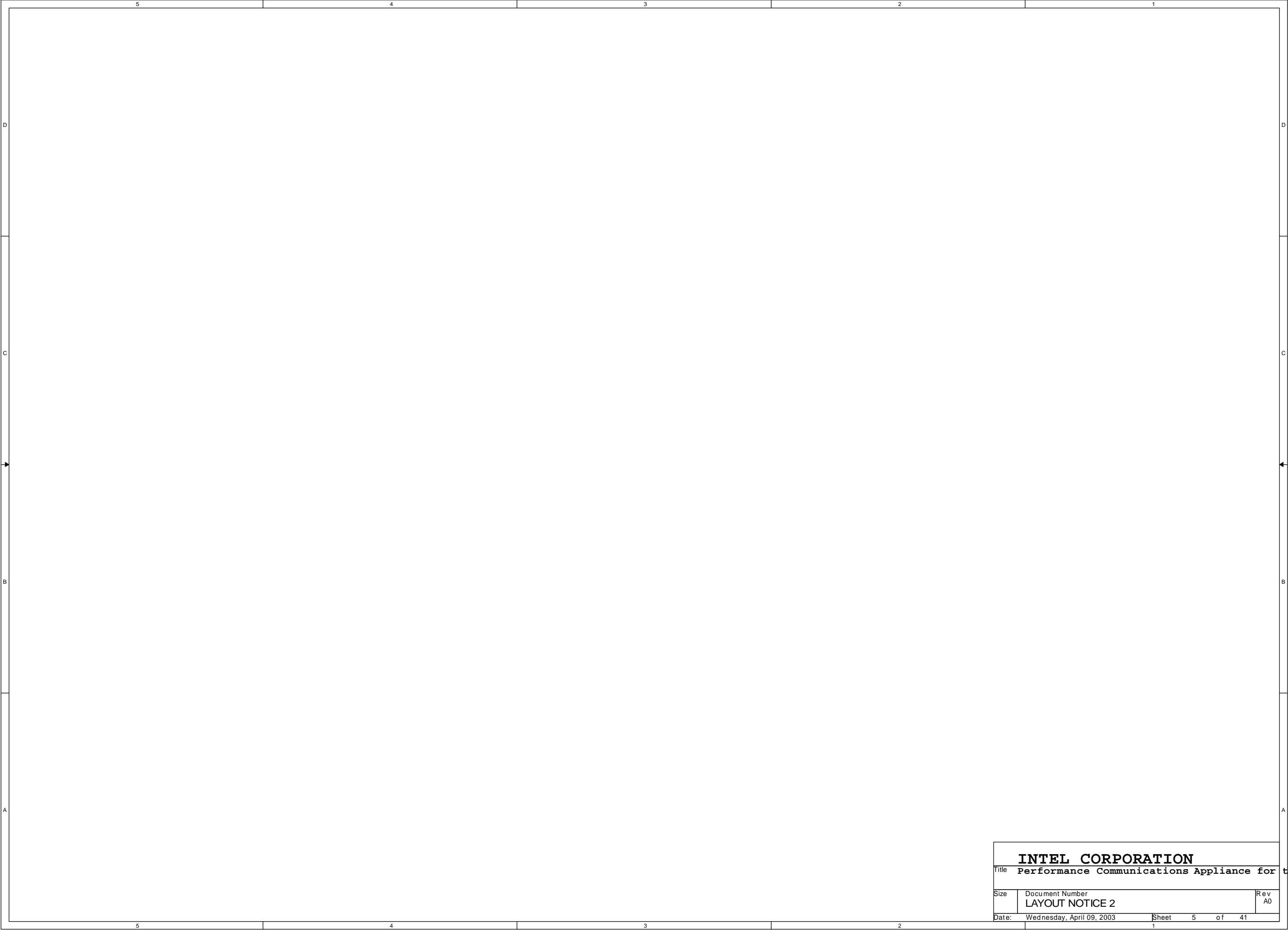
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INTERRUPT ROUTING TABLE:

ICH3 INTERRUPT:

PIRQA#: P64H2

PIRQB#: 82551 AD18

PIRQC#: 32BIT PCI SLOT

PIRQD#: NO USE

PIRQE#: NO USE

PIRQF#: NO USE

PIRQG#: NO USE

PIRQH#: NO USE

P64H2

P1AIRQ0: PCI-X SLOT P1A\_AD20

P1AIRQ1: PCI-X SLOT

P1AIRQ2: PCI-X SLOT

P1AIRQ3: PCI-X SLOT

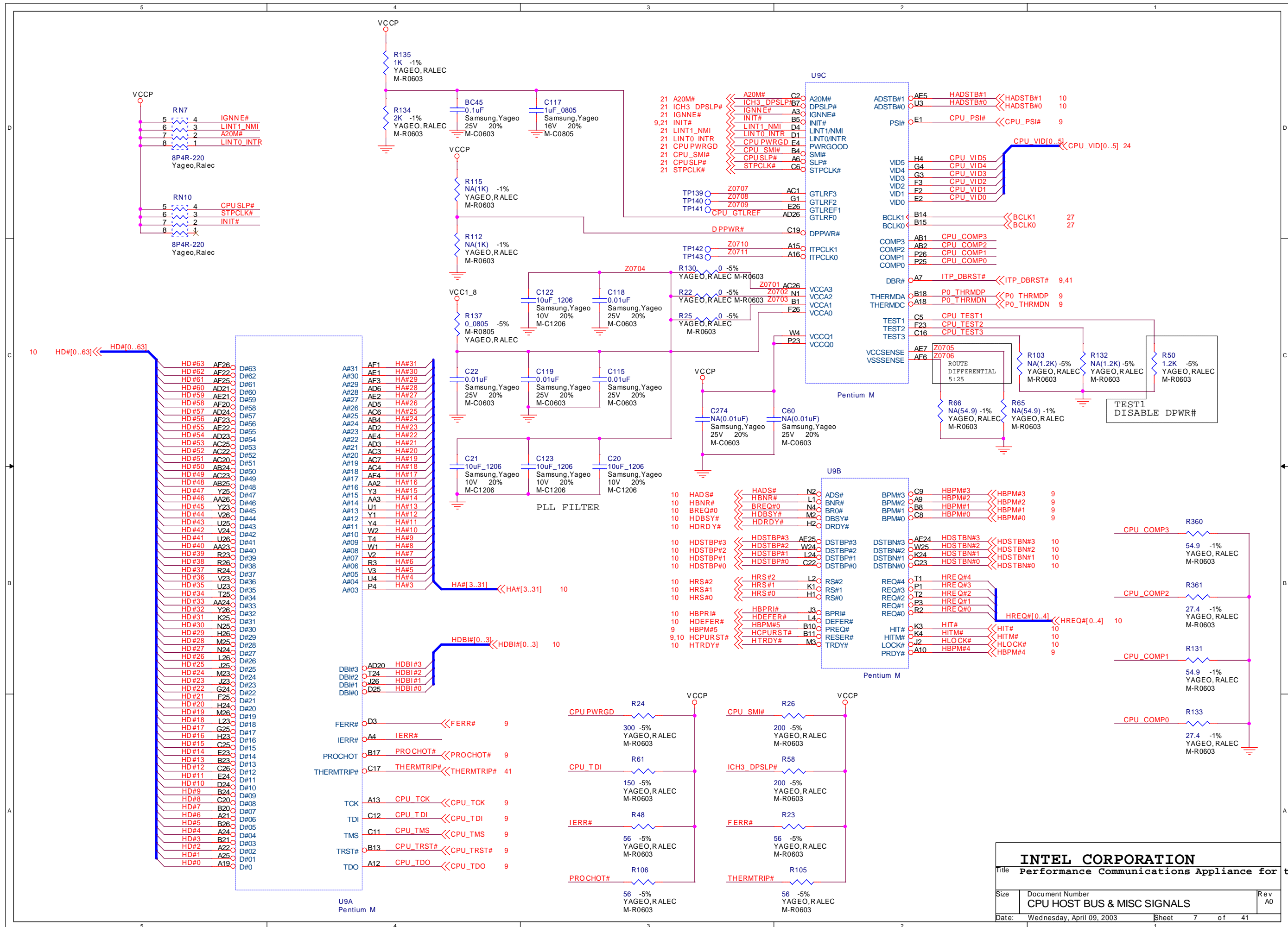
P1BIRQ0: 82546EB P1B\_AD20

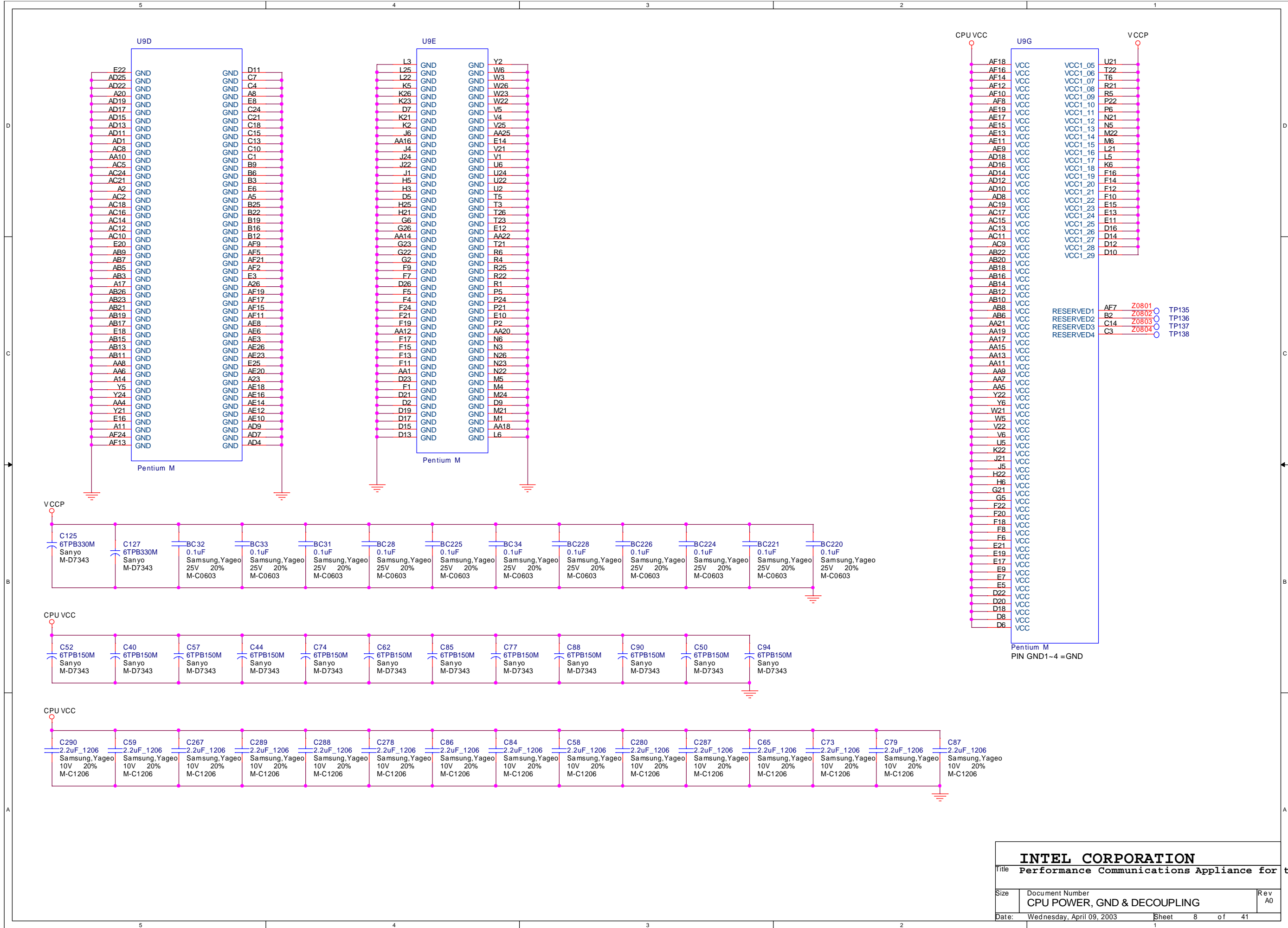
CONNECTOR:

CN1: 10/100M Bits RJ45  
CN2: 10/100/1000 bits RJ45  
CN3: 10/100/1000 bits RJ45  
CN4: COM1 Connector  
CN5: USB Connector  
CN6: PS/2 KB/MOUSE  
CN7: COM2 Connector  
CN8: CPU FAN Power Connector  
CN9: Auxiliary +12V Power  
CN10: ITP700FLEX Connector  
CN11: ATX Power  
CN12: SYSTEM FAN Power Connector  
CN13: Connector for LEDs, RESET Button, POWER Button  
CN14: FLOPPY DRIVE Connector  
CN15: PRIMARY IDE Connector  
CN16: SECONDARY IDE Connector  
CN17: SYSTEM FAN Power Connector  
SW1: Power Button  
SW2: Reset Button  
SLOT1: 32Bits PCI Slot  
SLOT2: PCI-X Slot  
MTH1: Hook for MCH Heat Sink  
MTH2: Hook for MCH Heat Sink

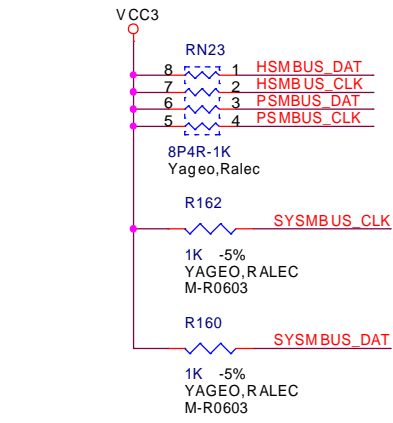
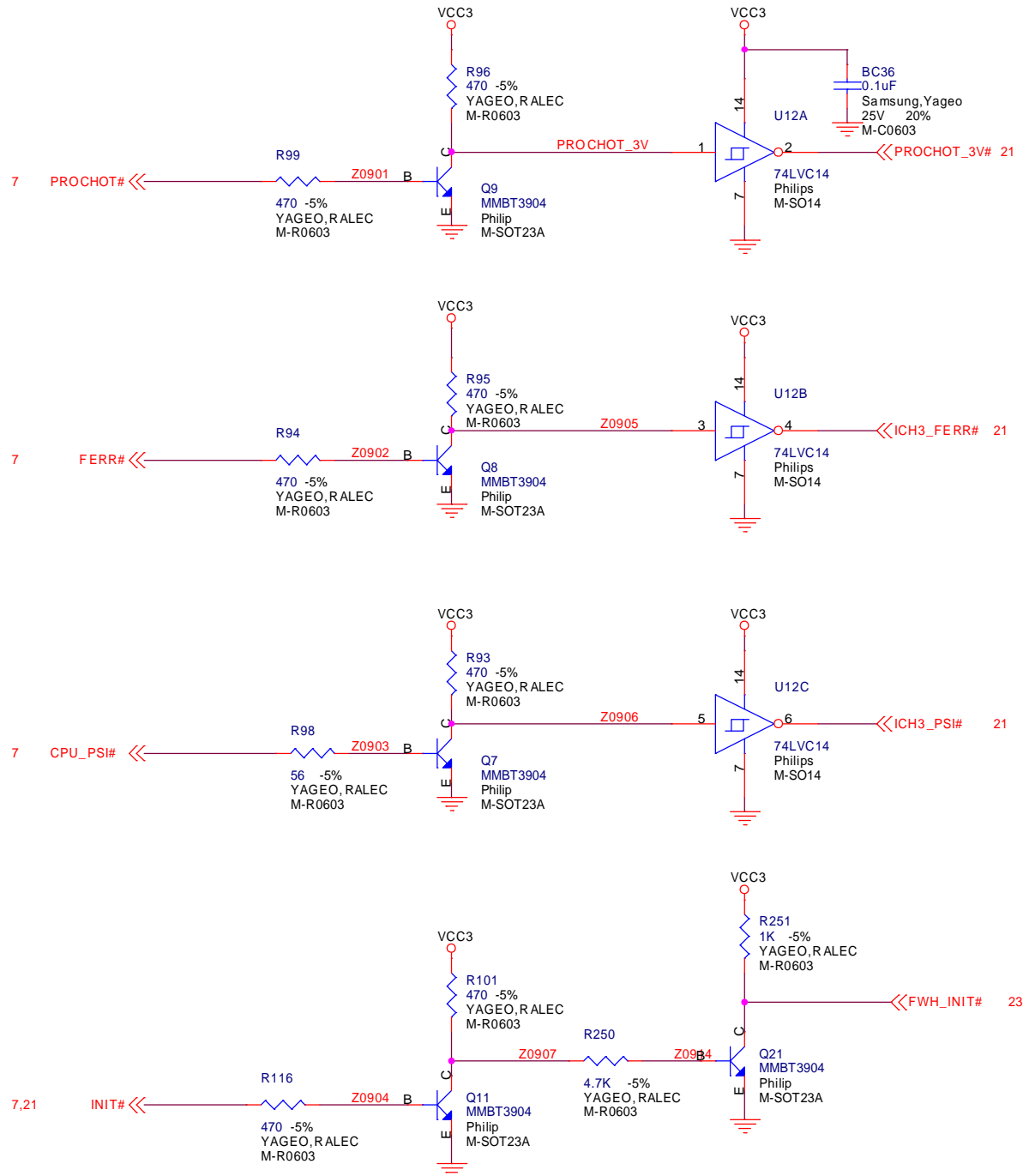
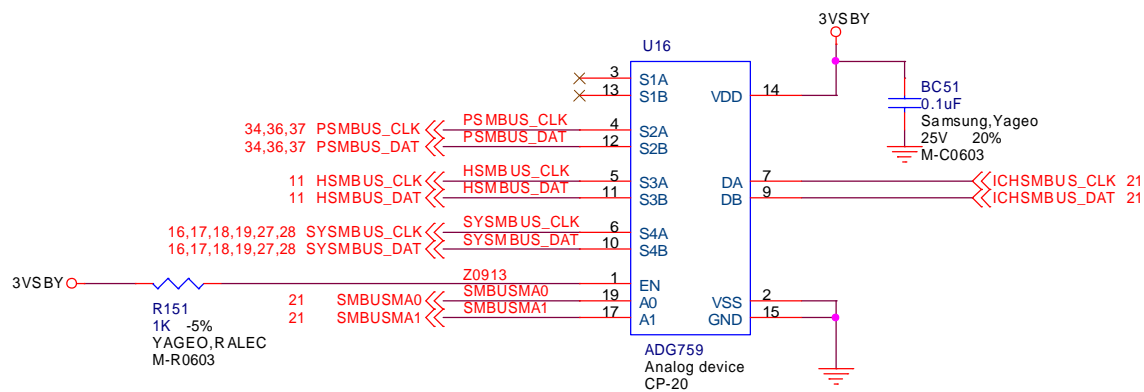
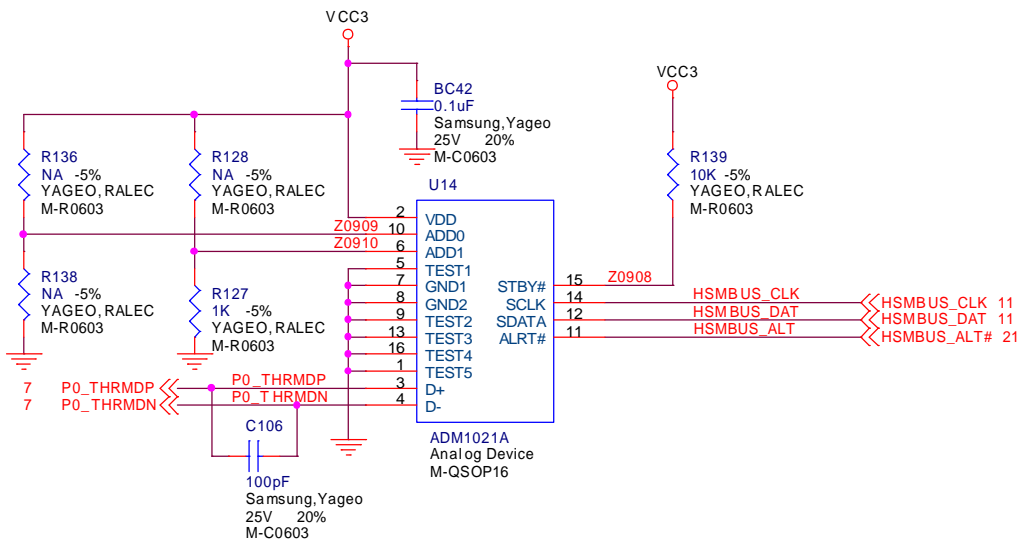
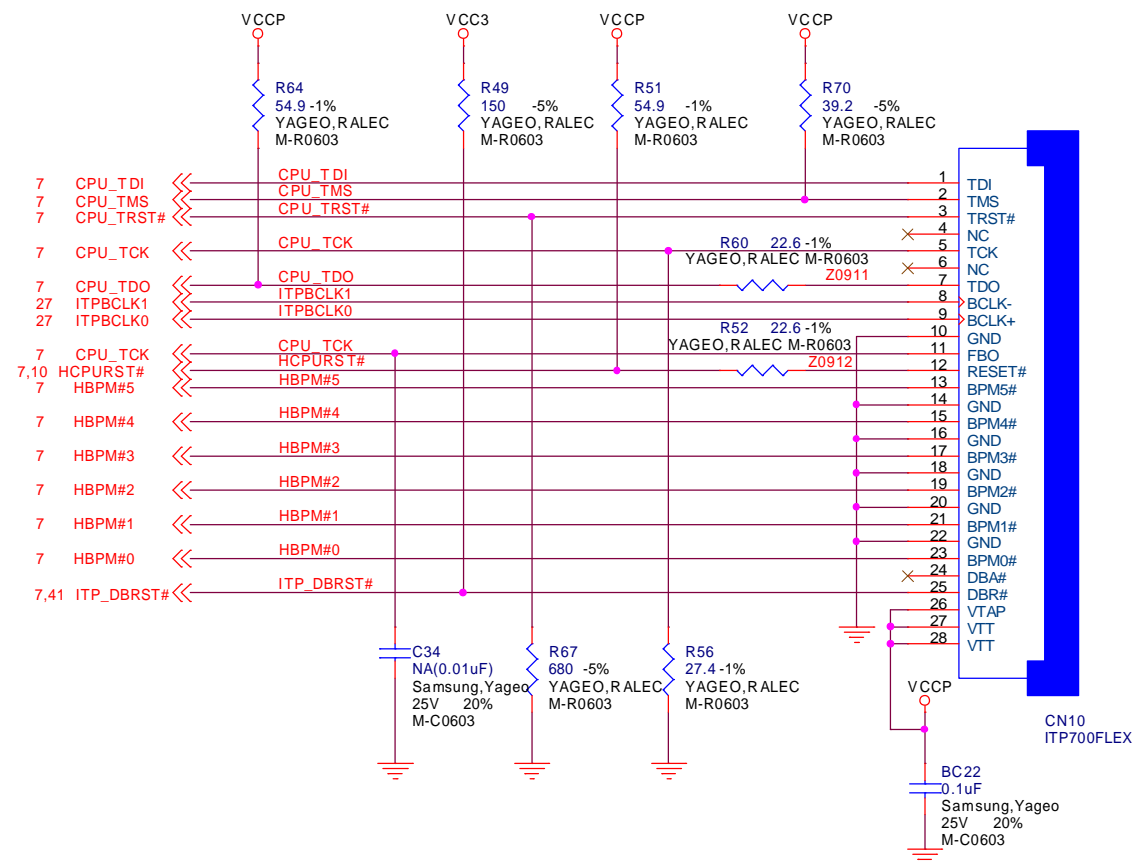
JUMPER:

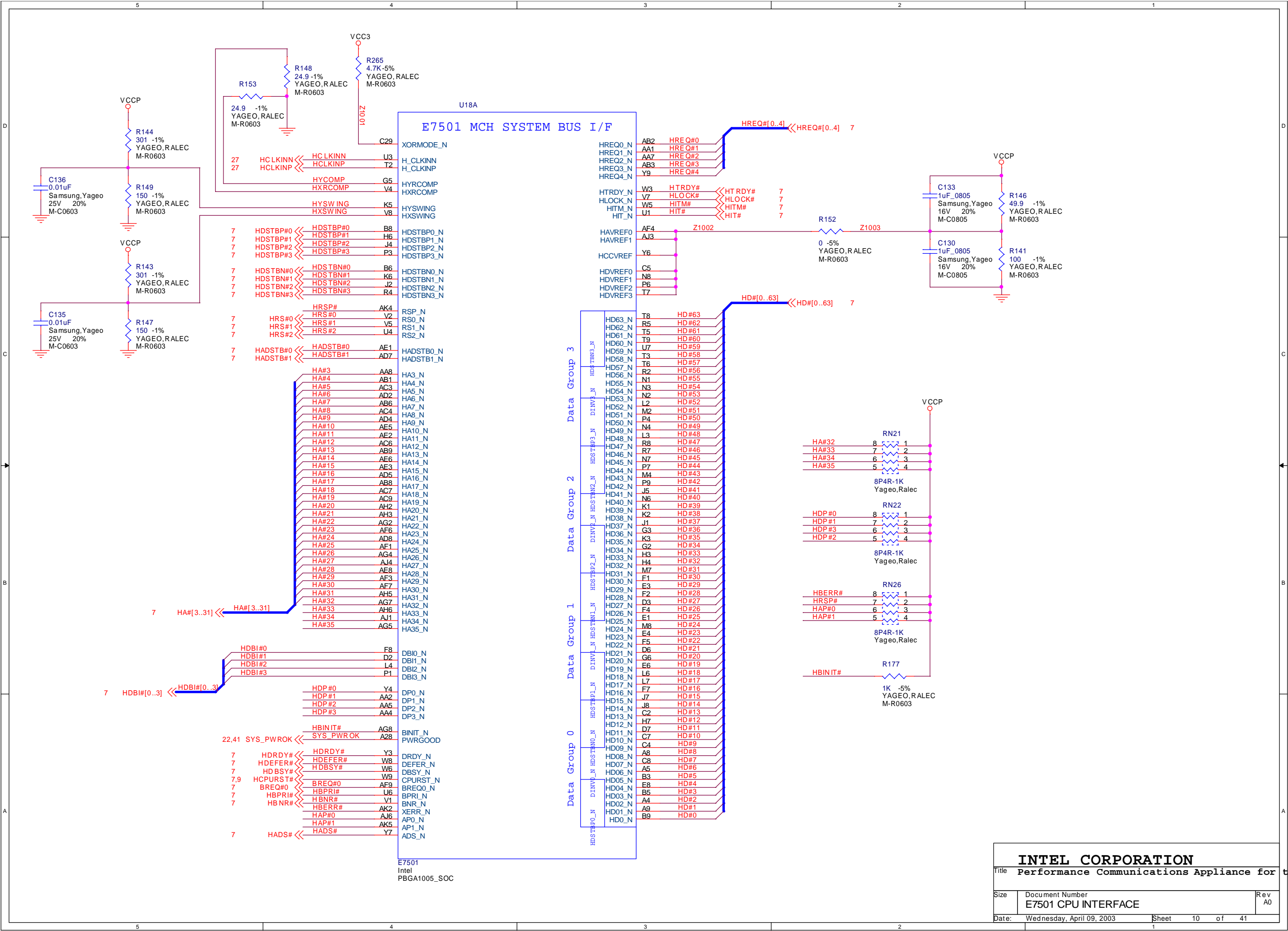
JP1, JP2, JP3: PCI-X SETTING  
  
JP4: BIOS WRITE PROTECT  
ON WRITE ENABLE  
OFF WRITE PROTECT  
  
JP5: TCO REBOOT  
ON NO REBOOT MODE  
OFF NORMAL  
  
JP6: BUZZER  
ON ENABLE  
OFF DISABLE  
  
JP7: TOP SWAP  
ON ENABLE  
OFF DISABLE  
  
JP8: CPU SAFE MODE  
ON DISABLE  
OFF ENABLE  
  
JP9: CMOS CLEAR  
1-2 NORMAL  
2-3 CLEAR

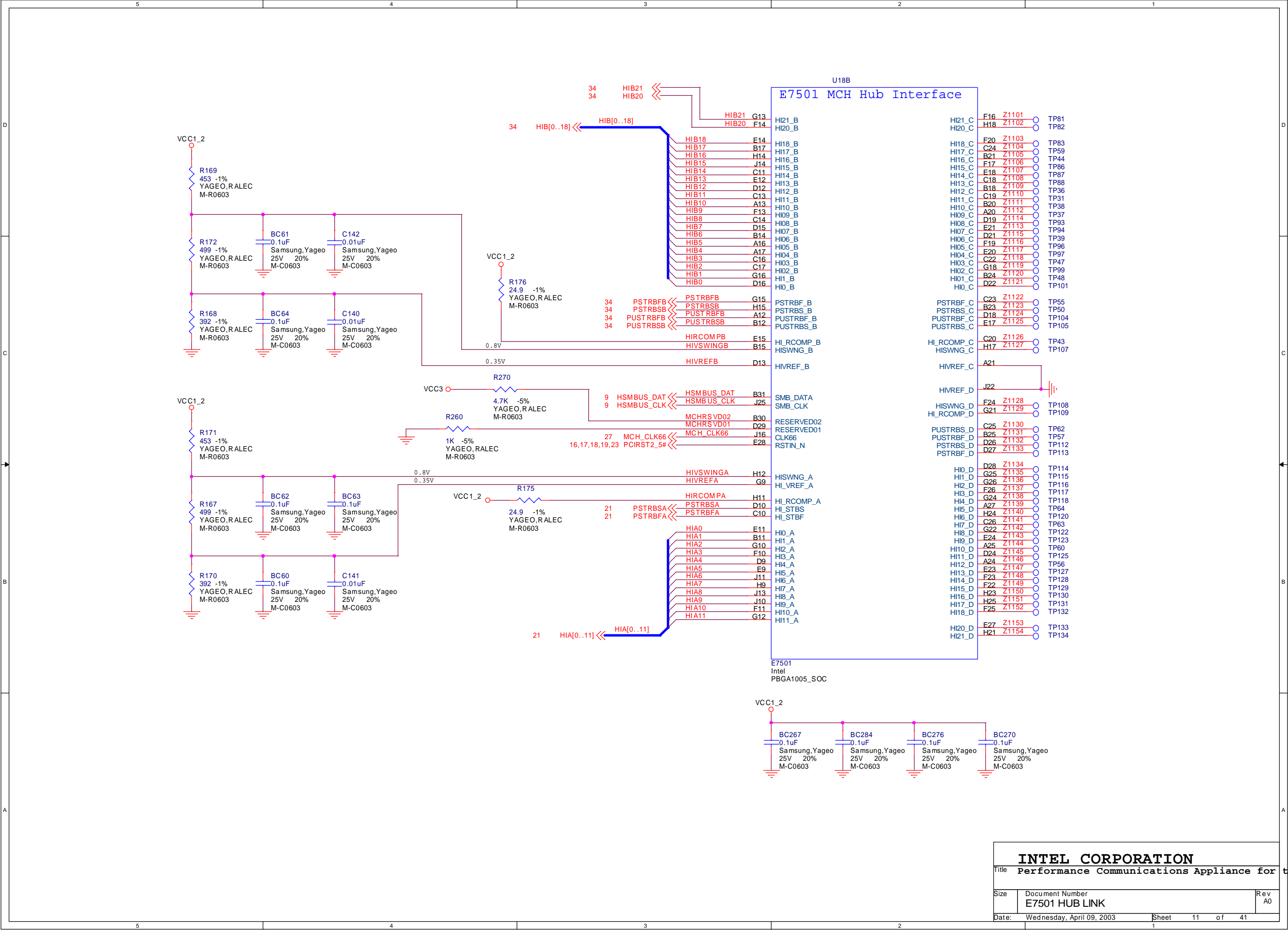


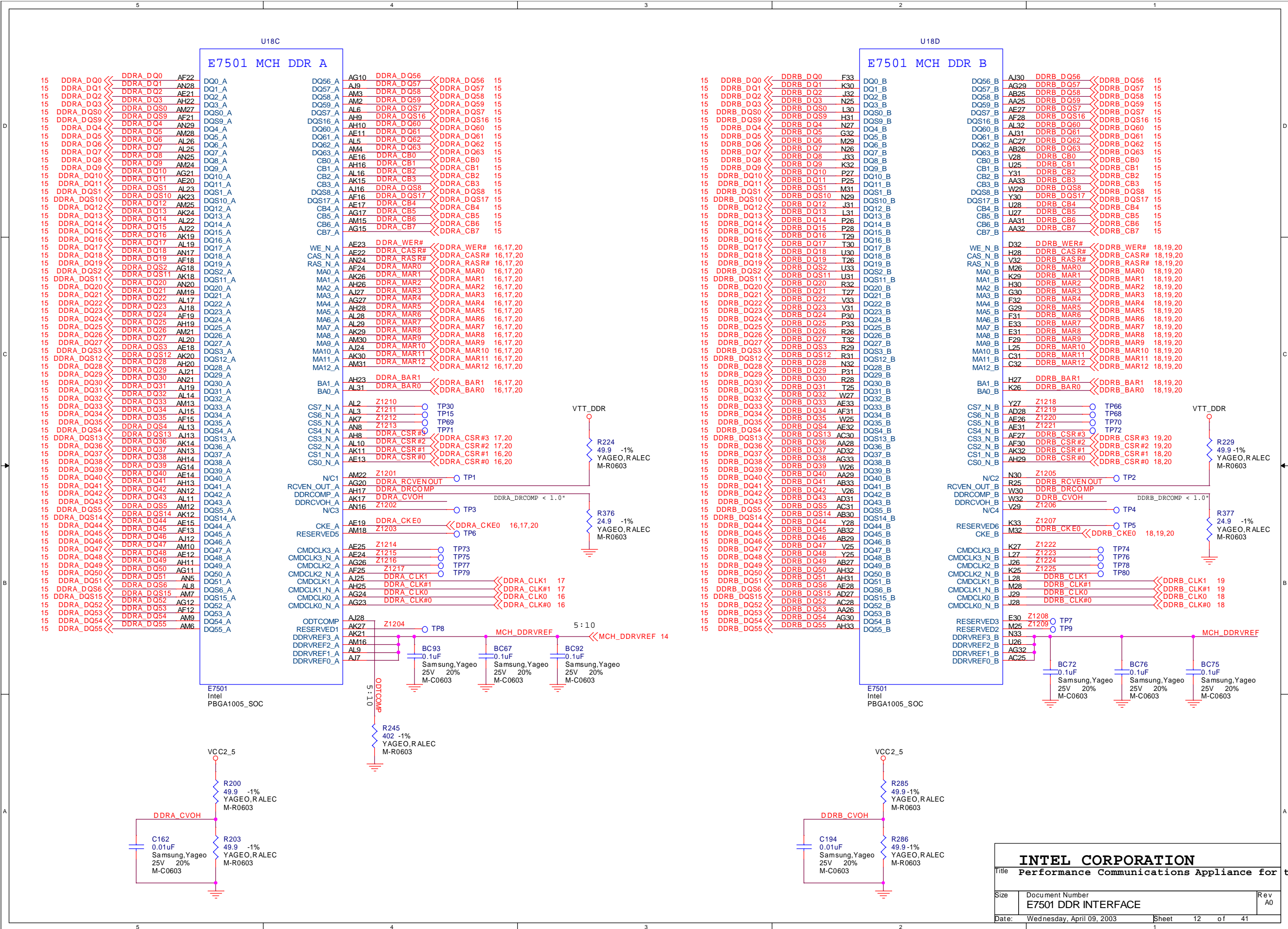






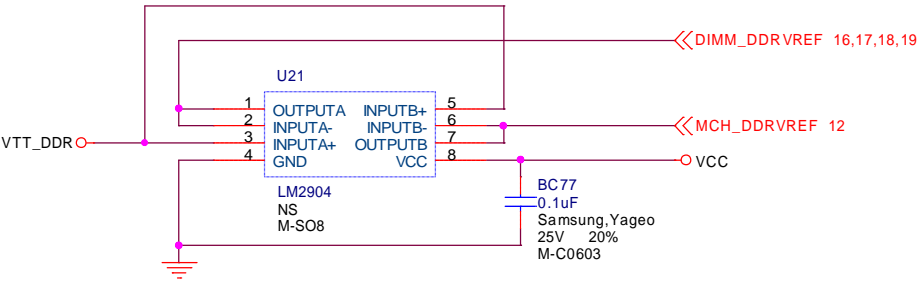
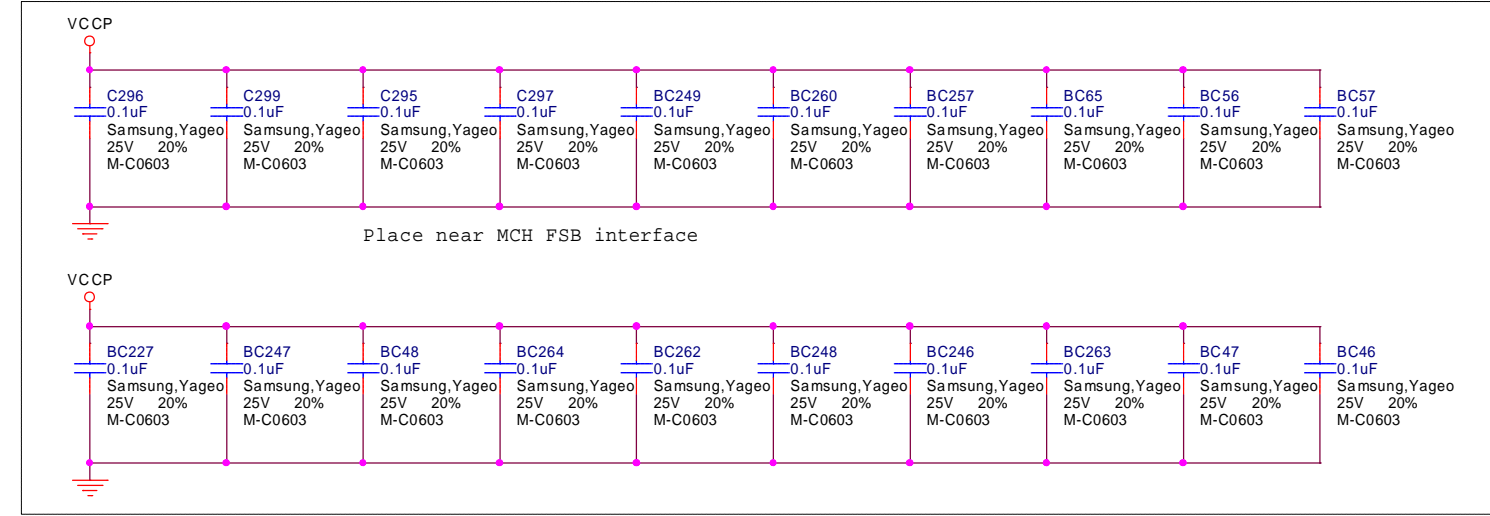
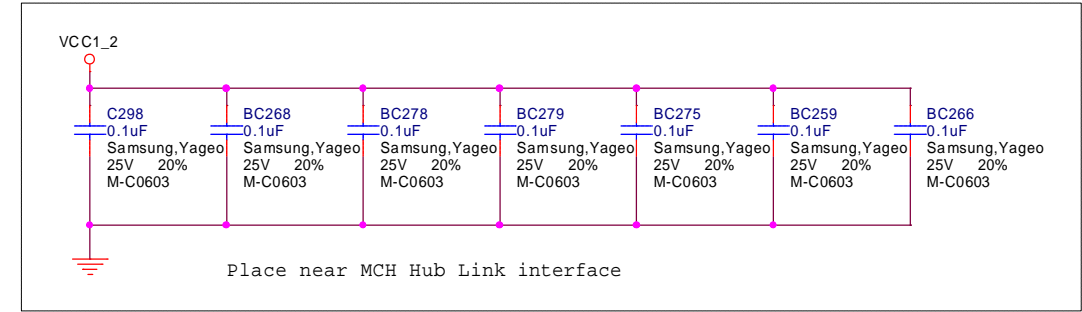
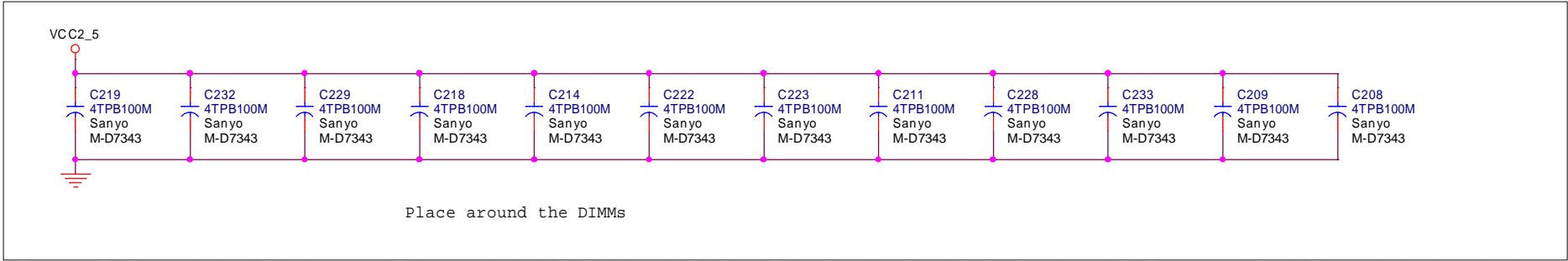
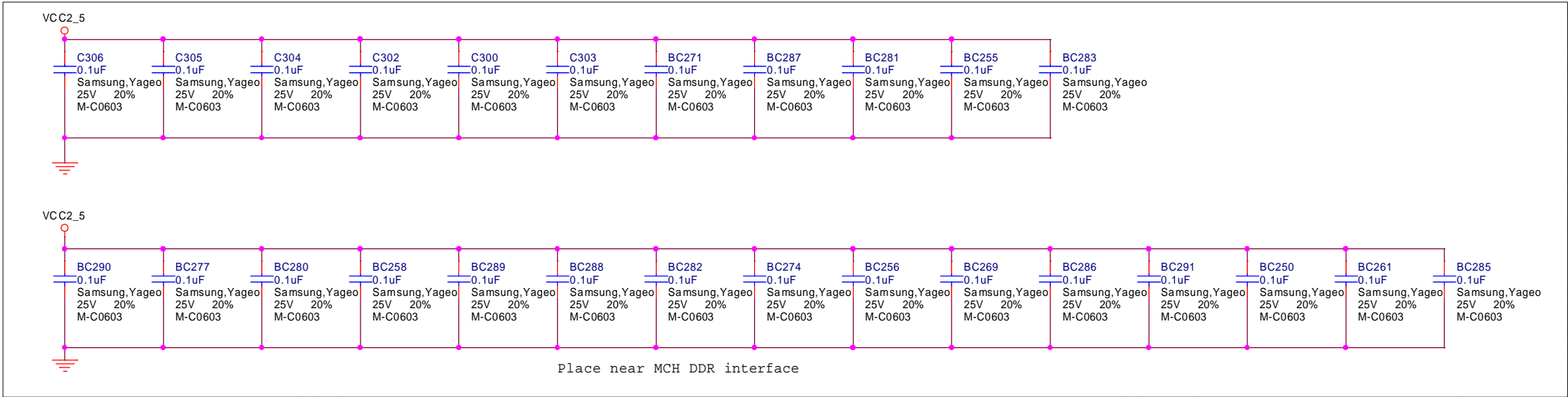


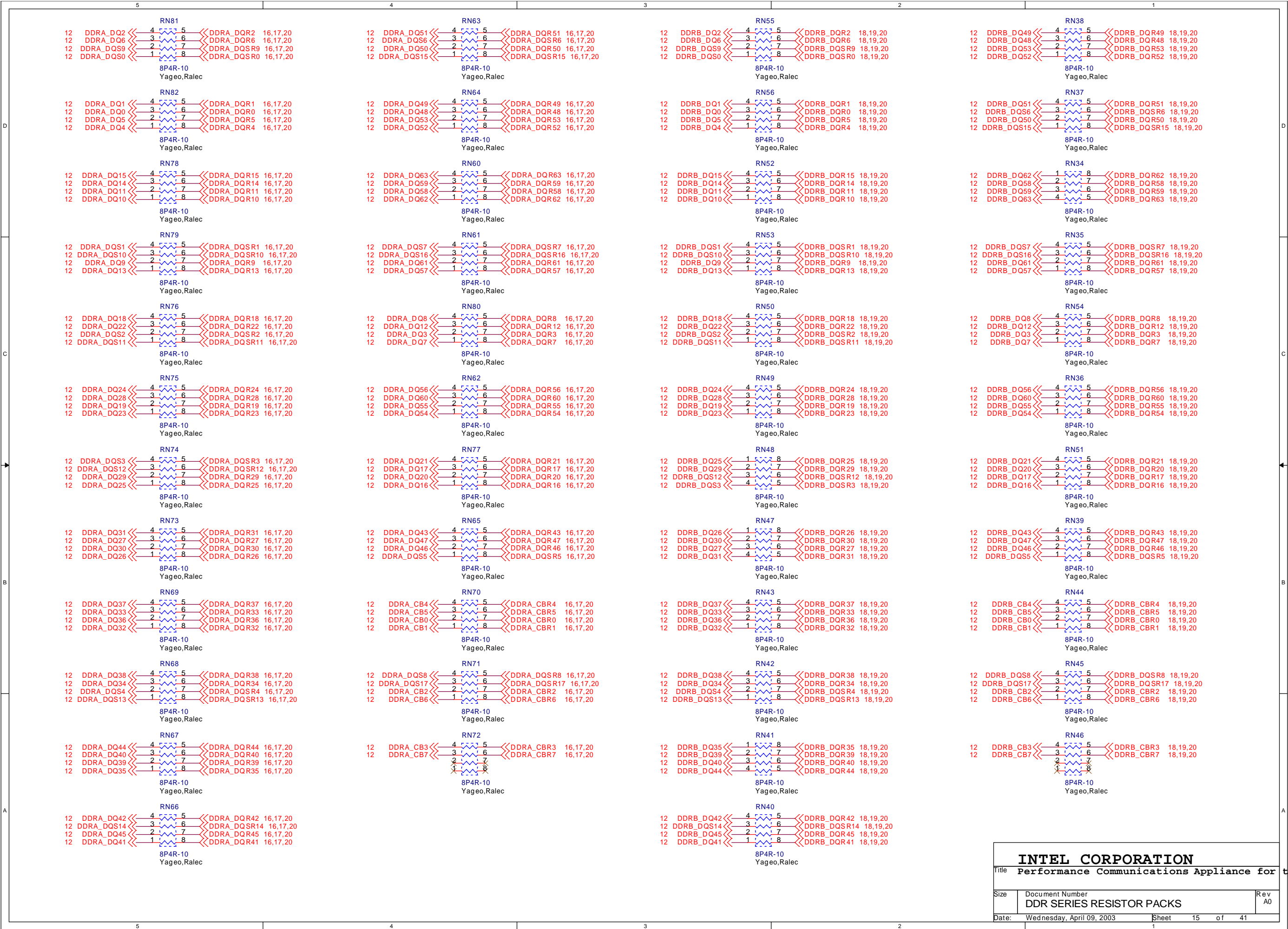


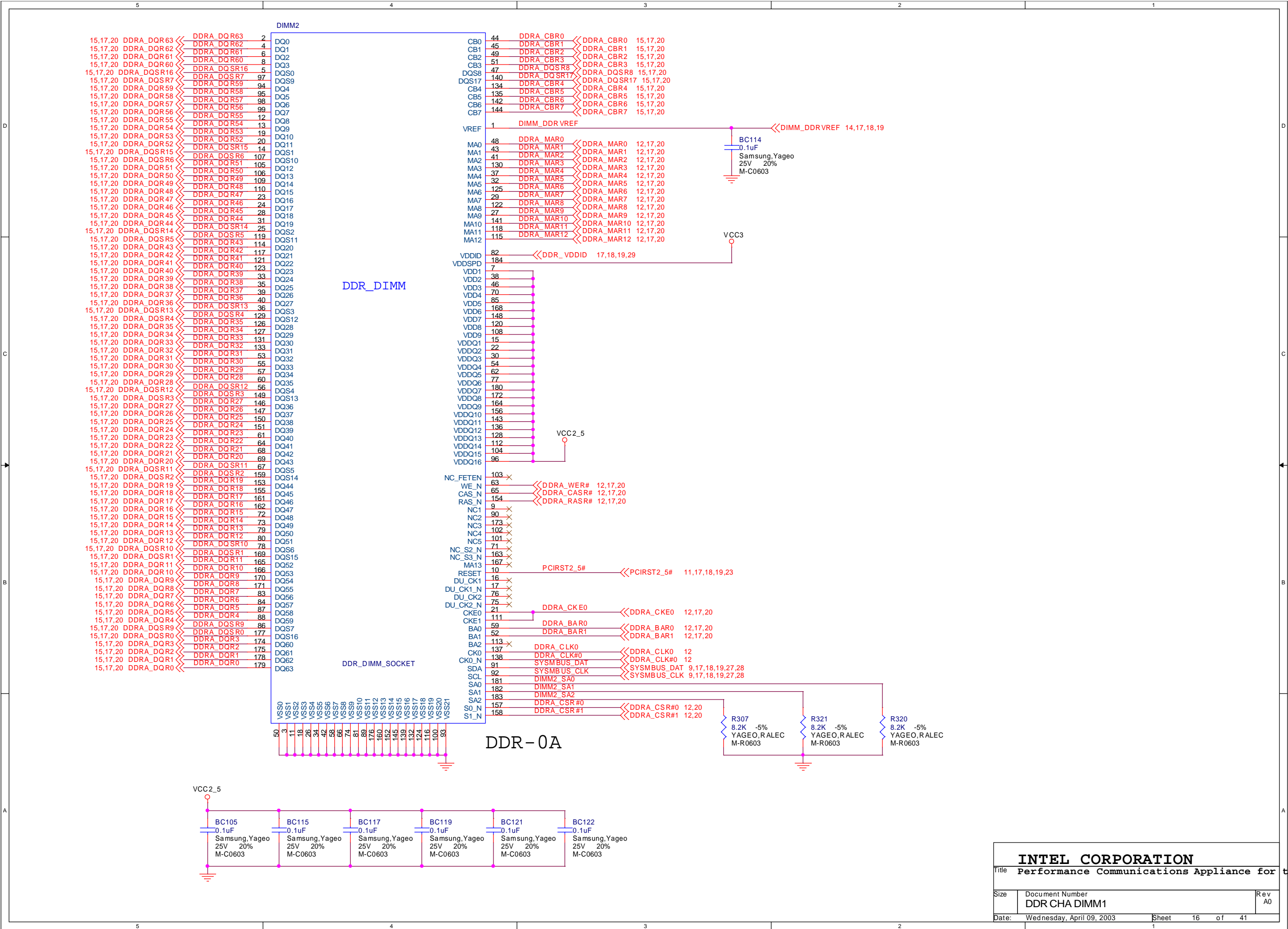




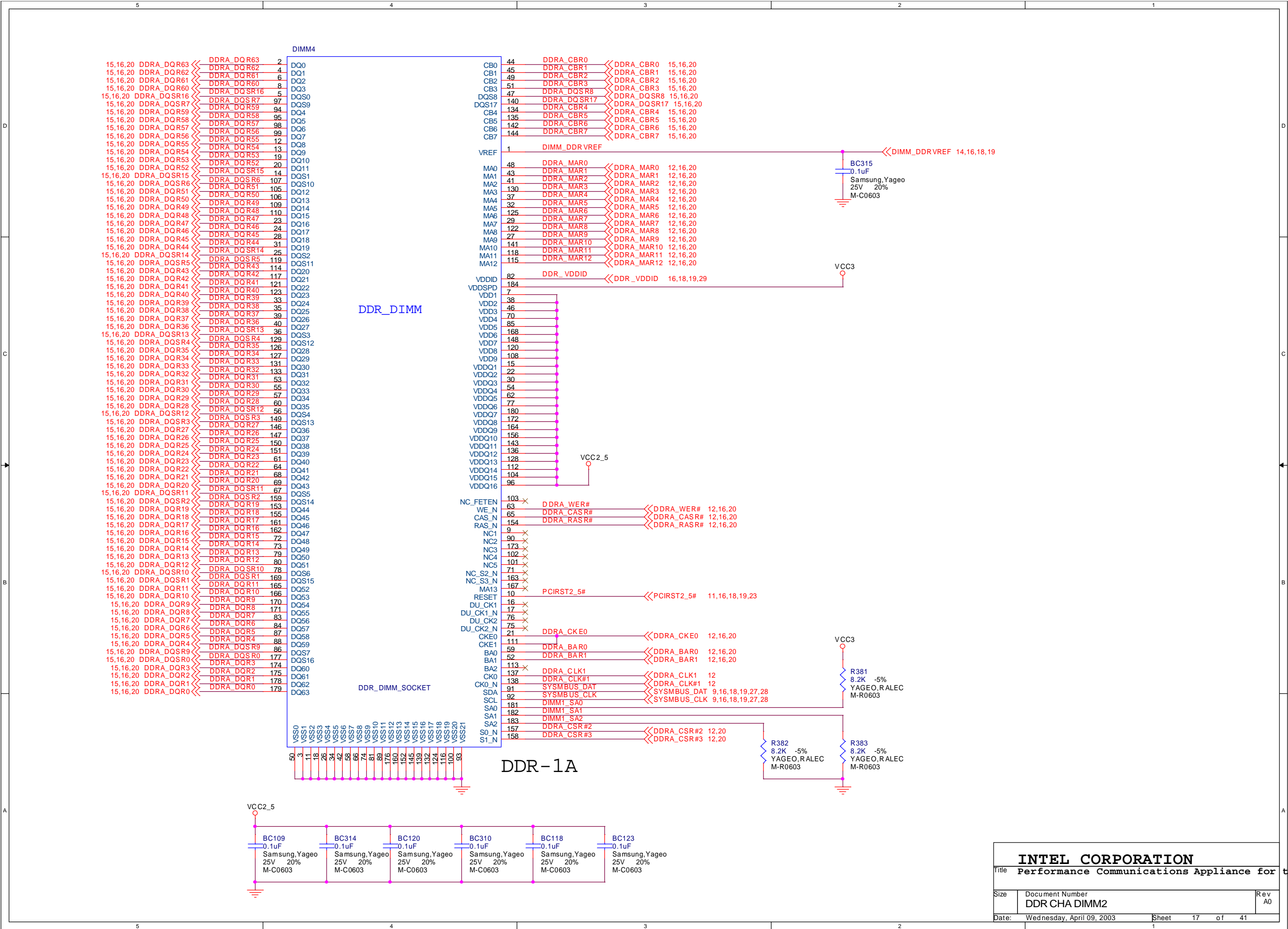


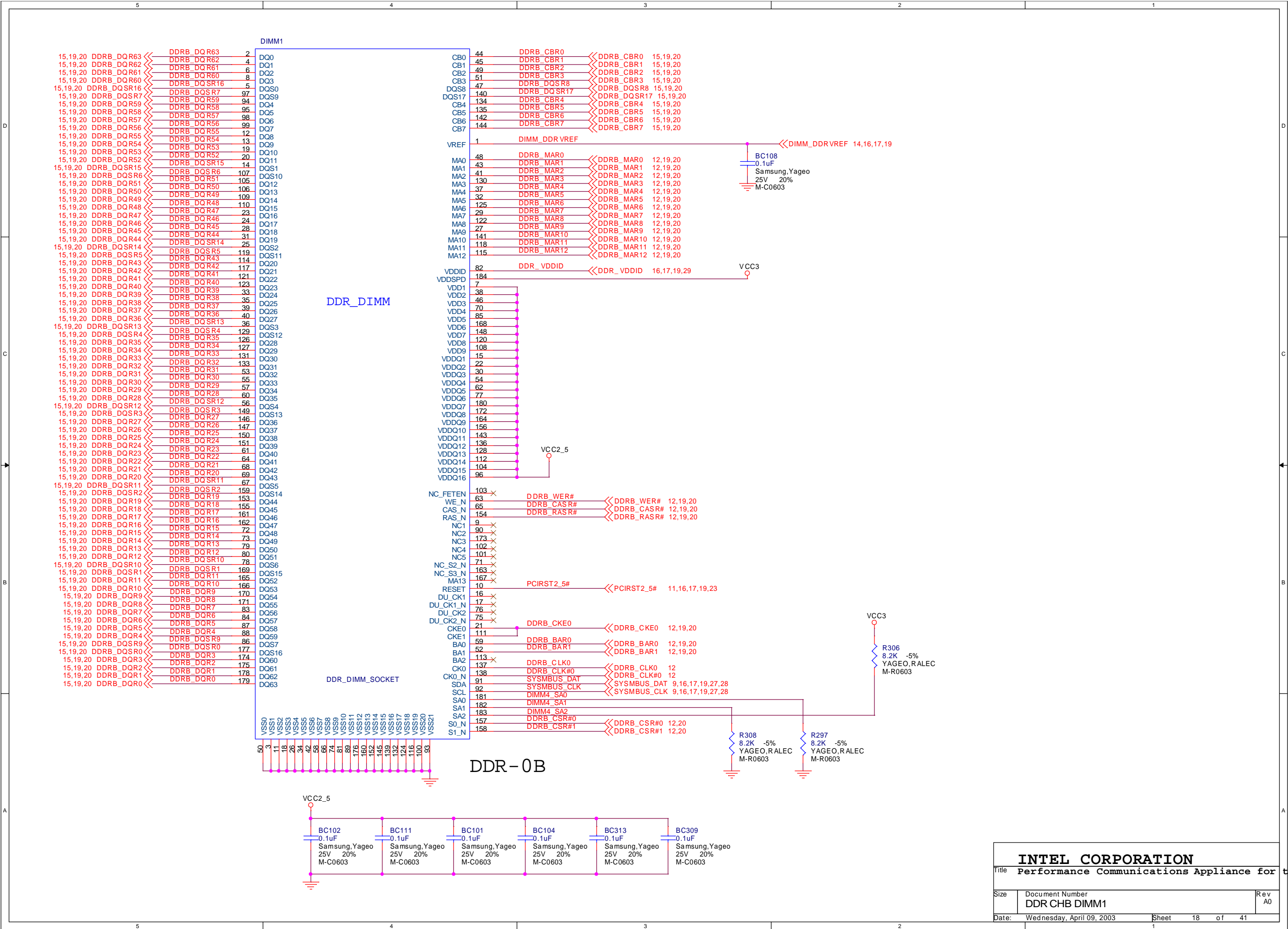


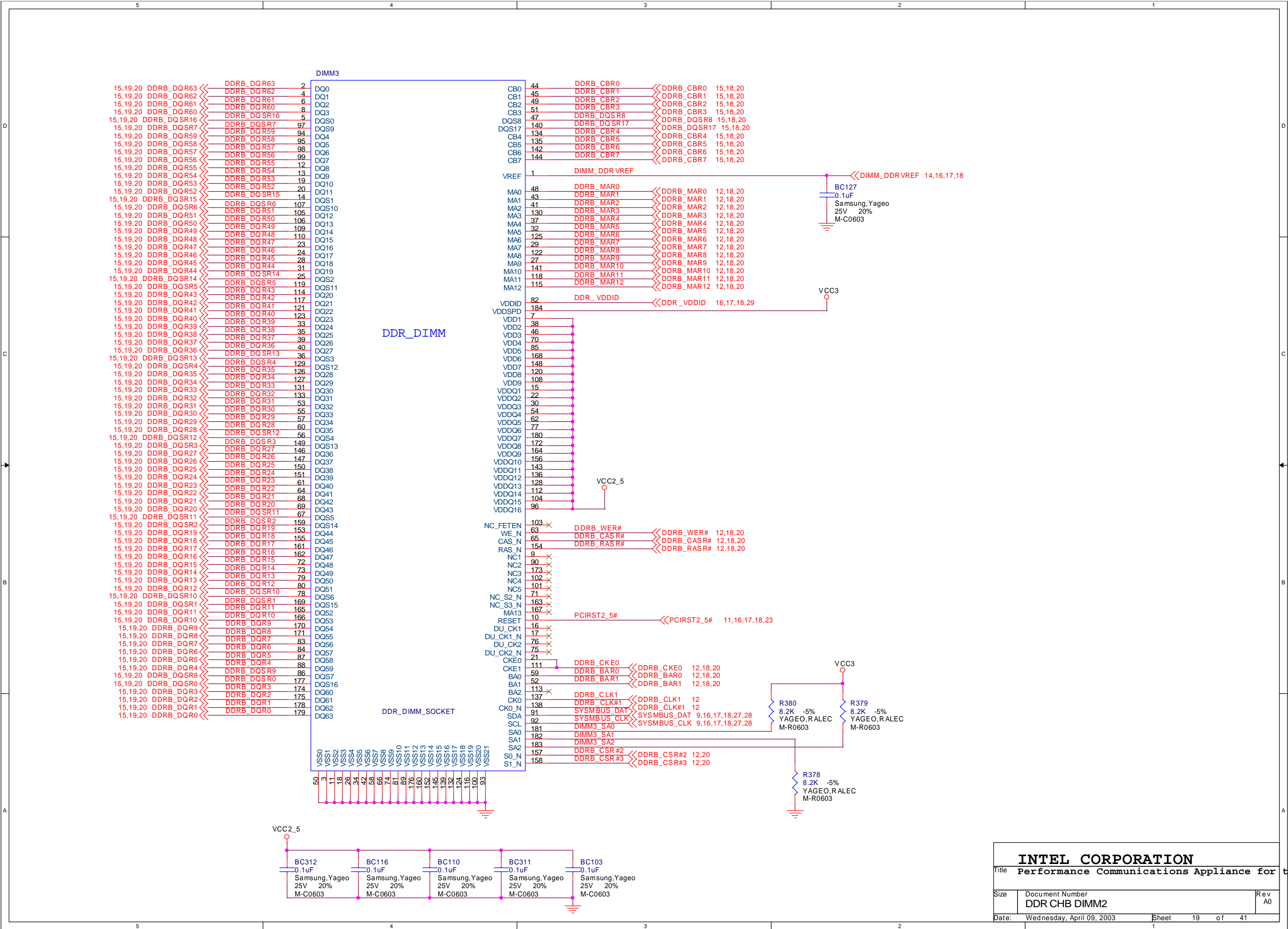






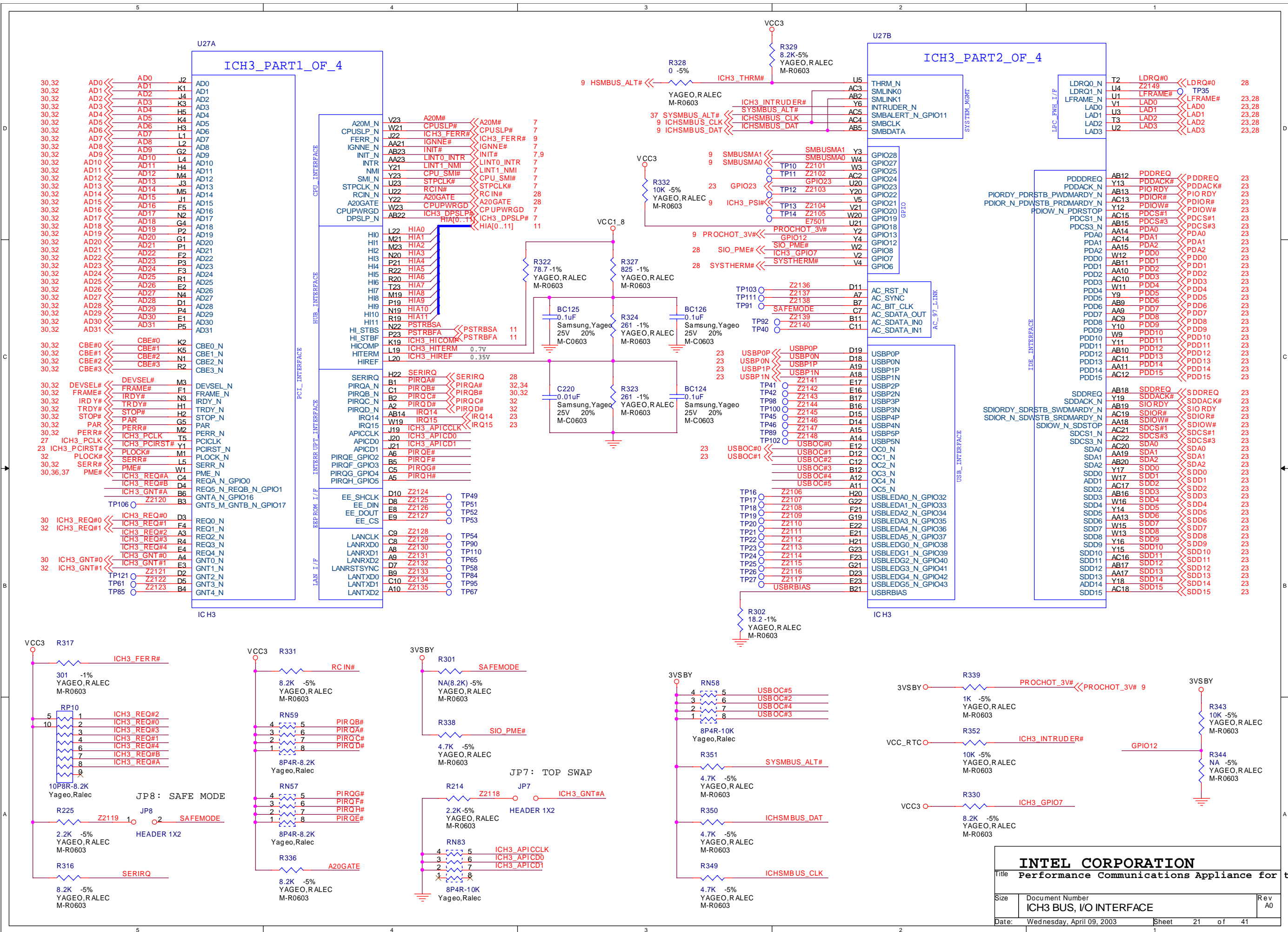


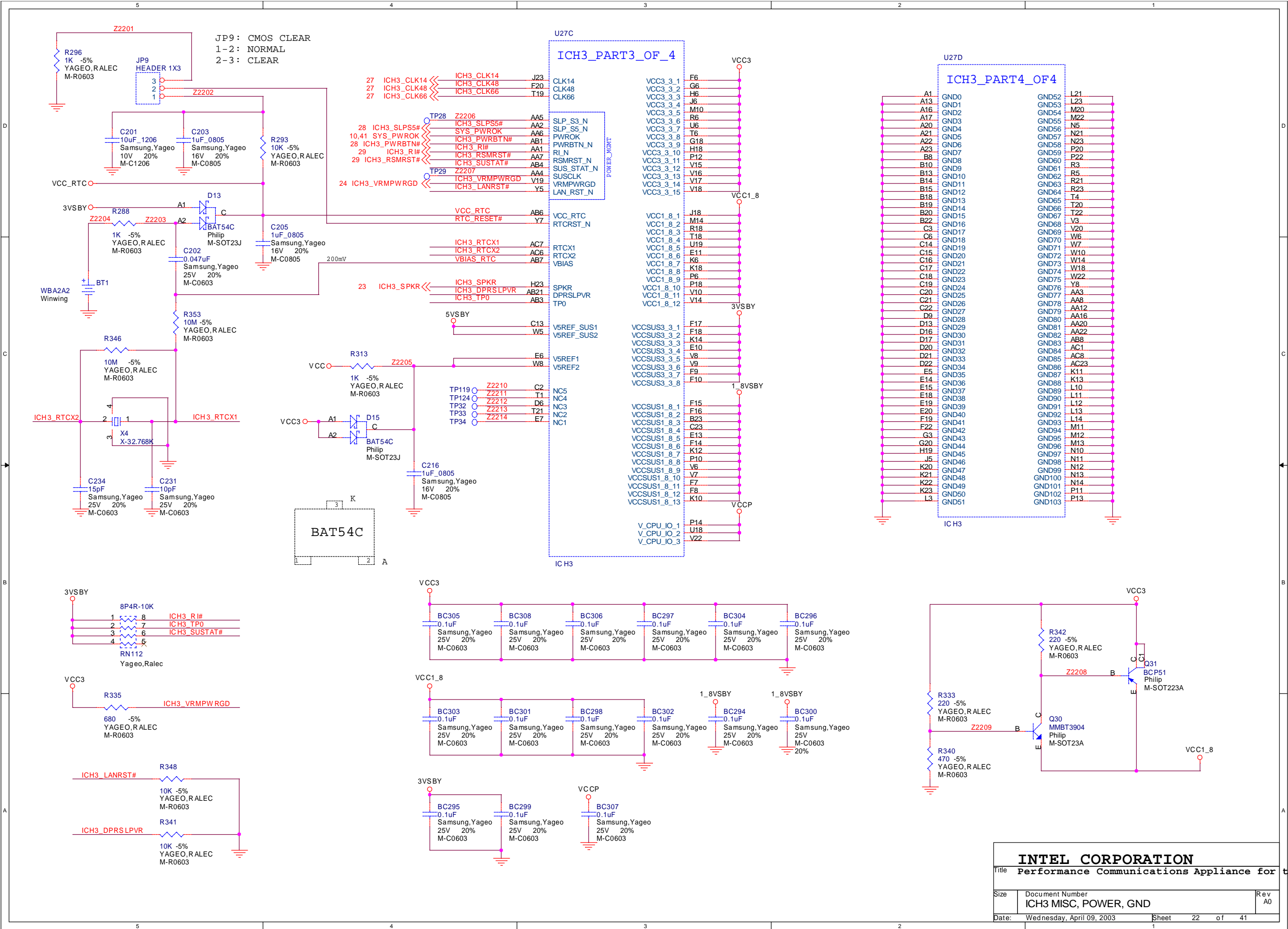


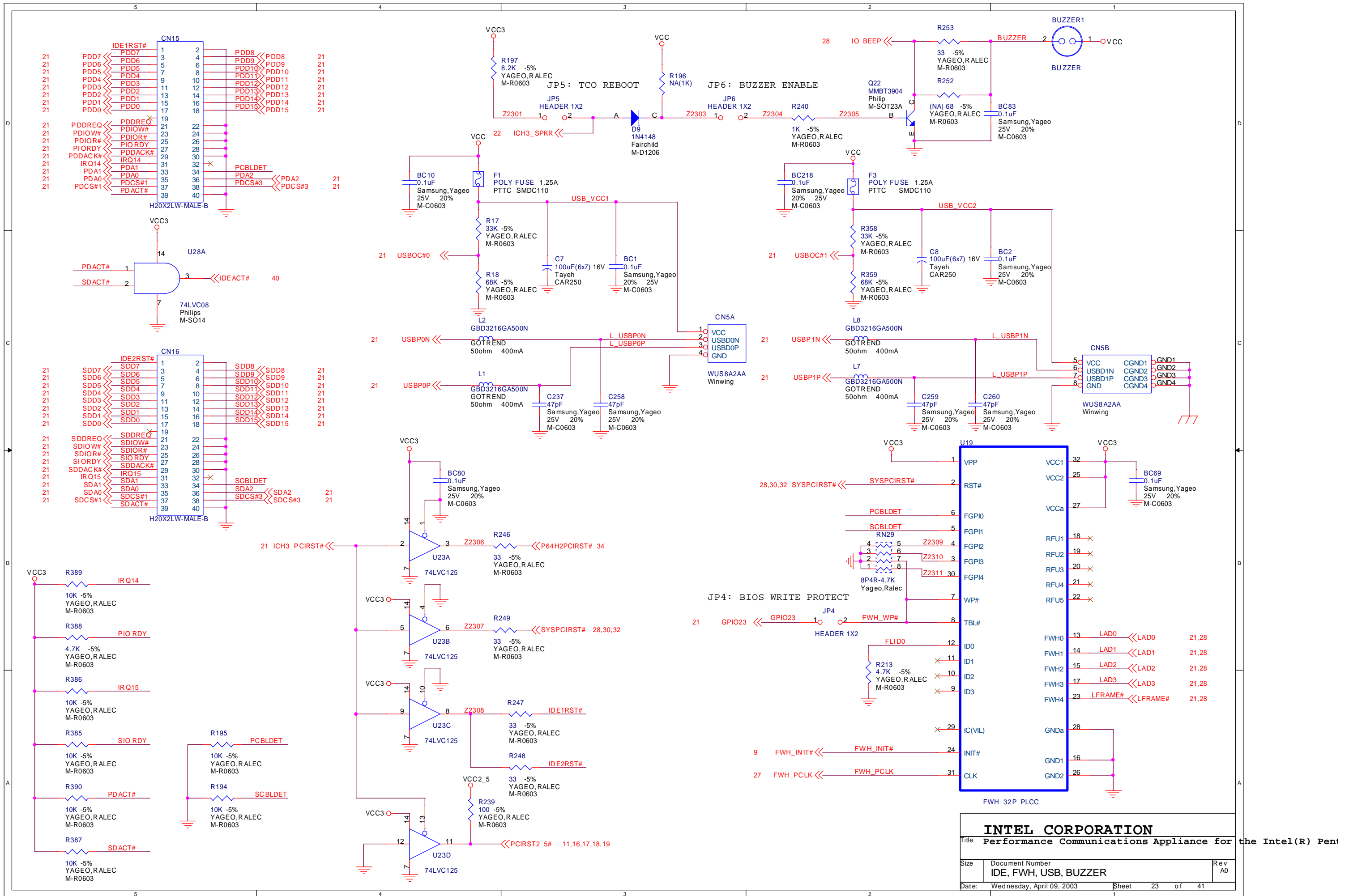






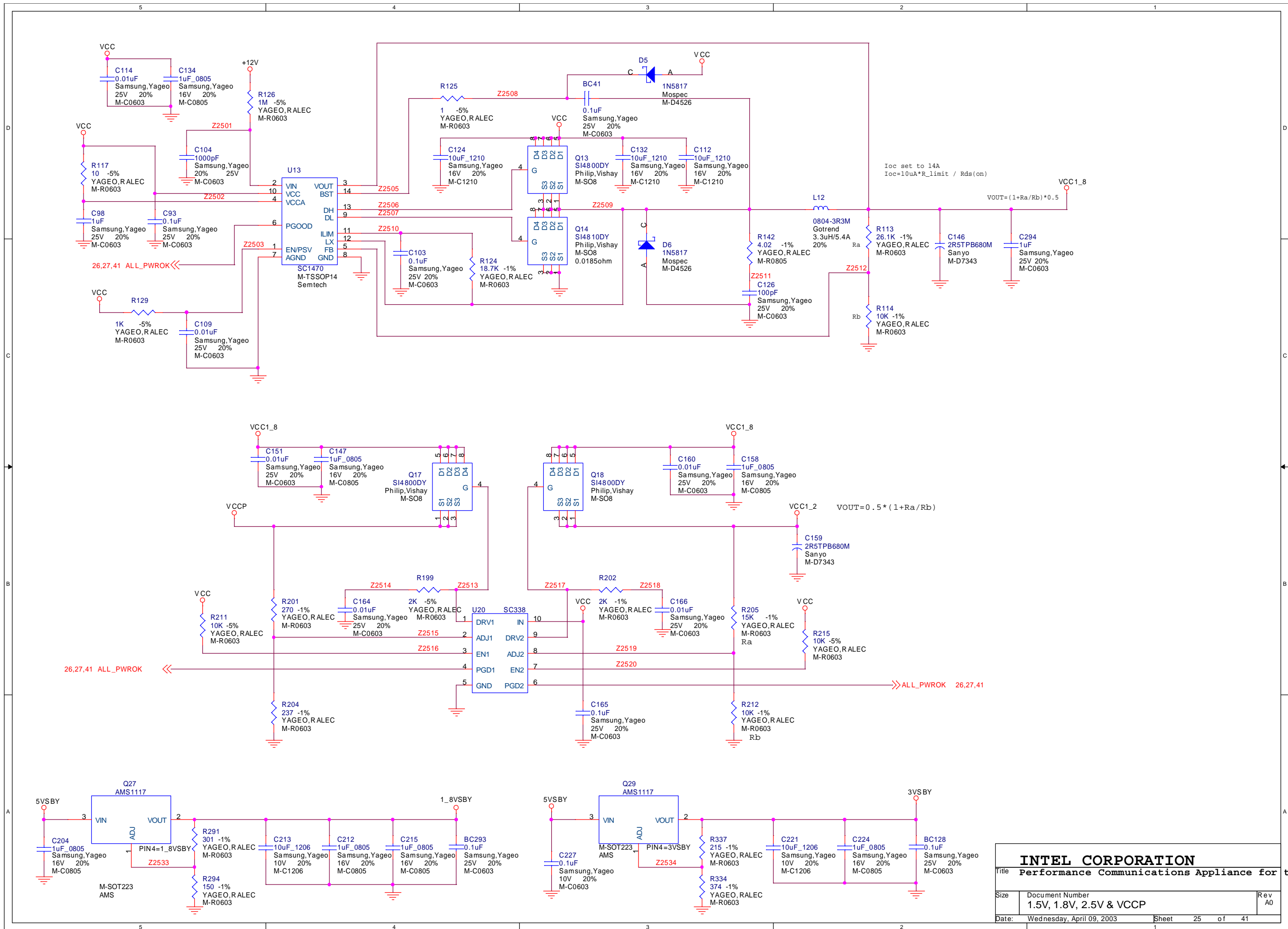




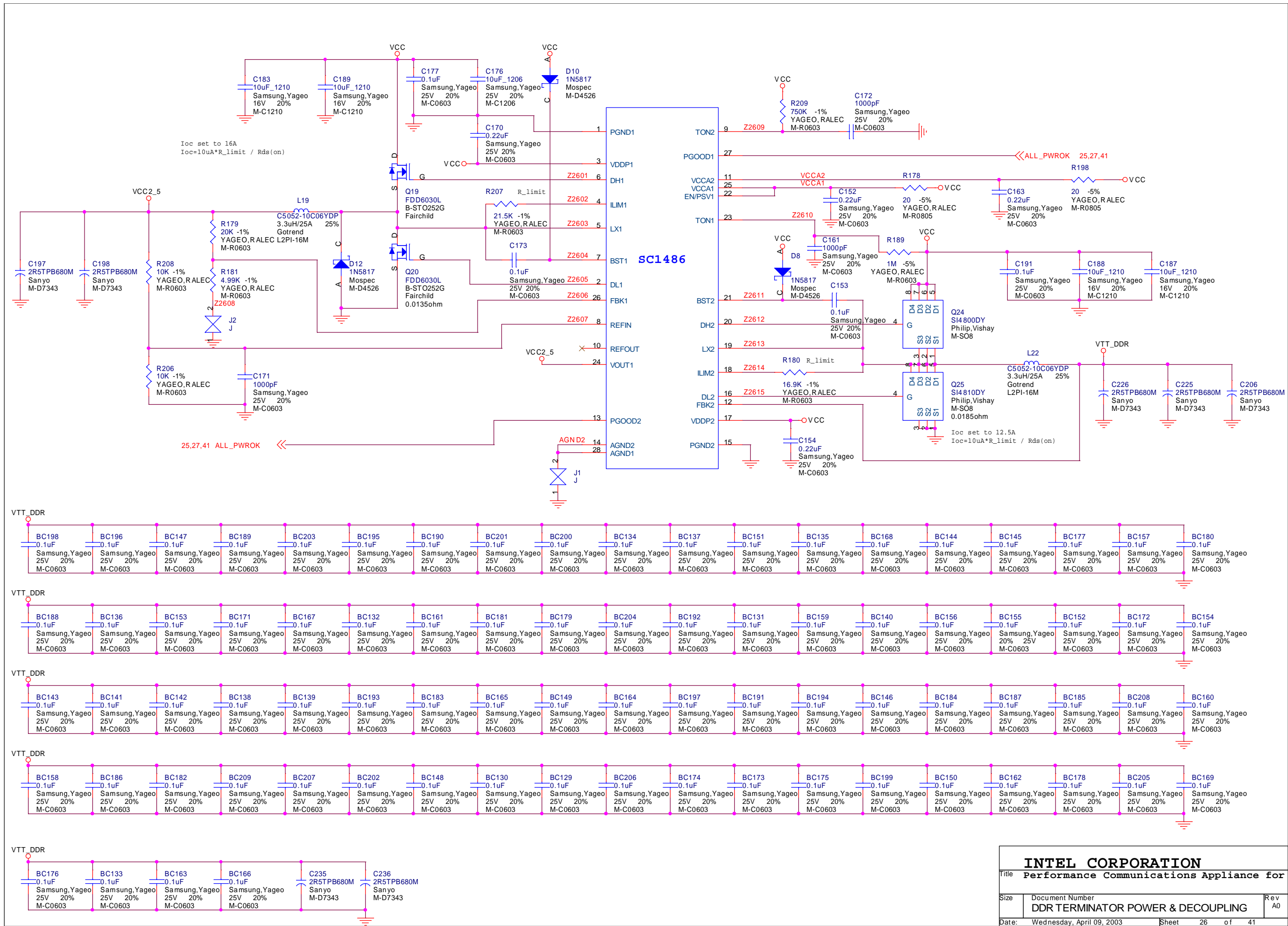


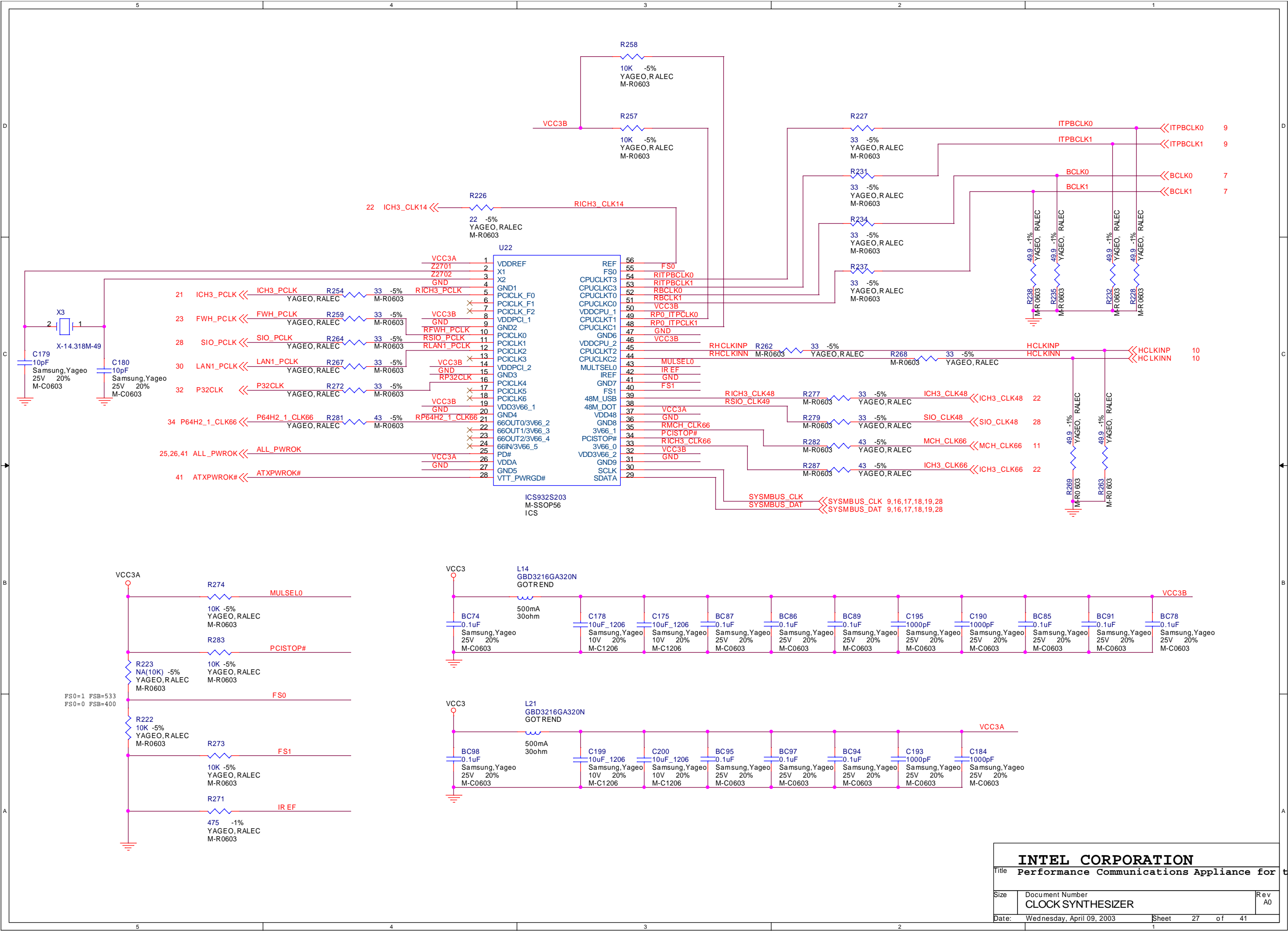


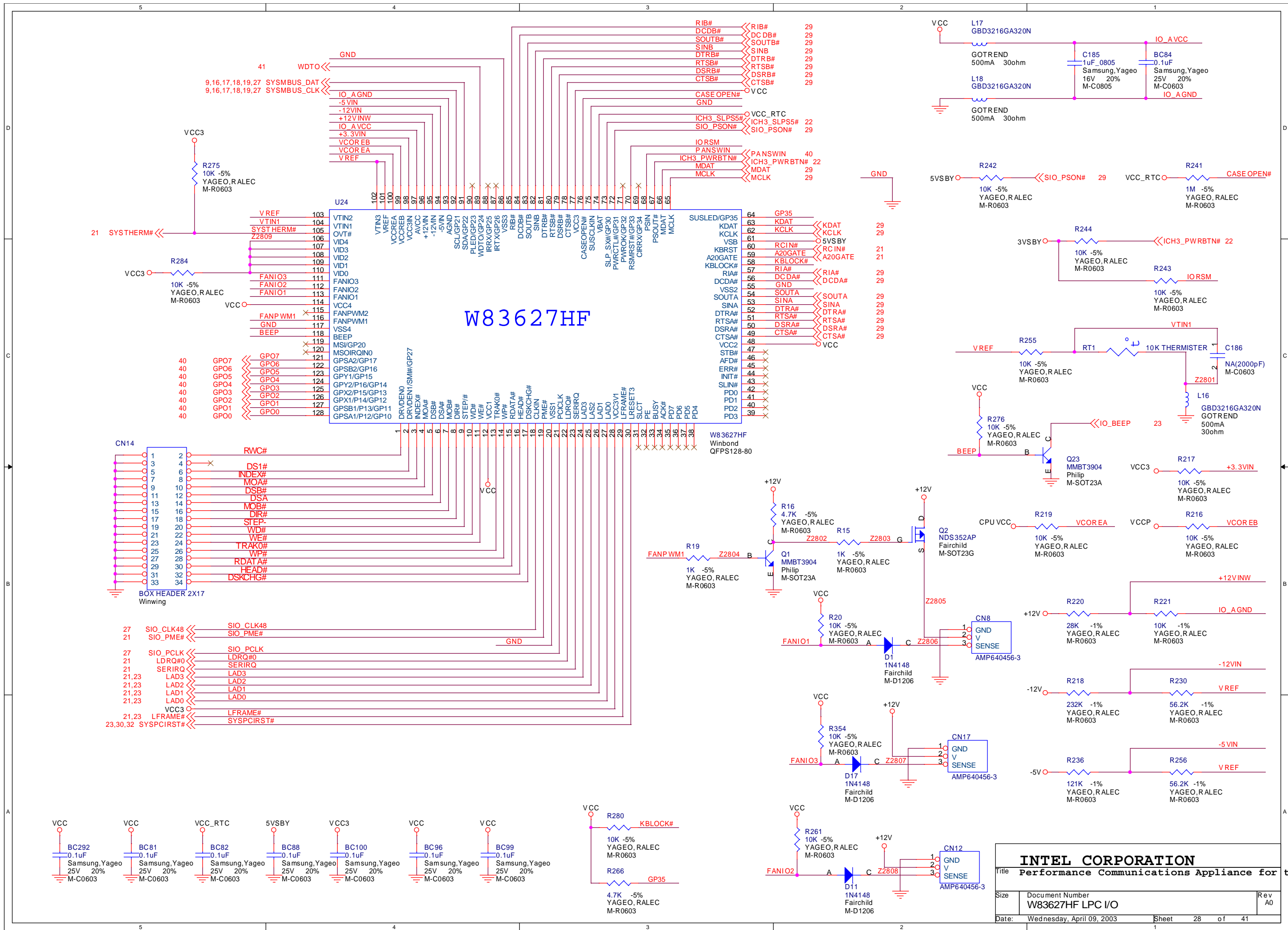


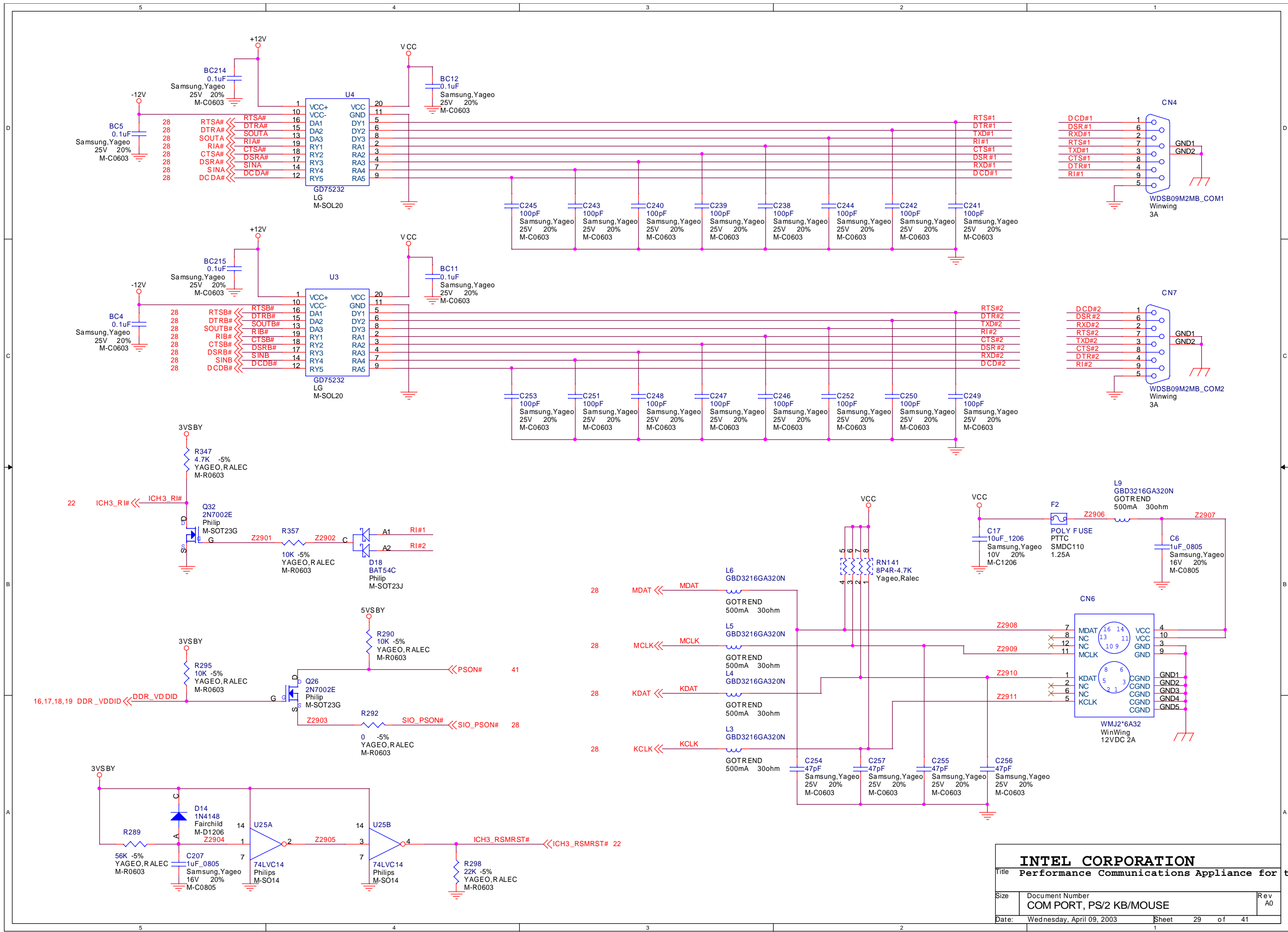


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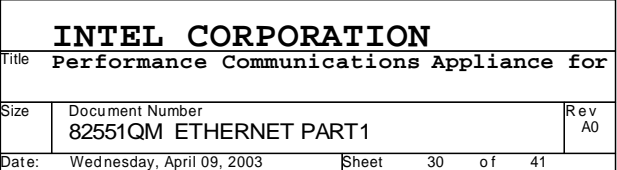


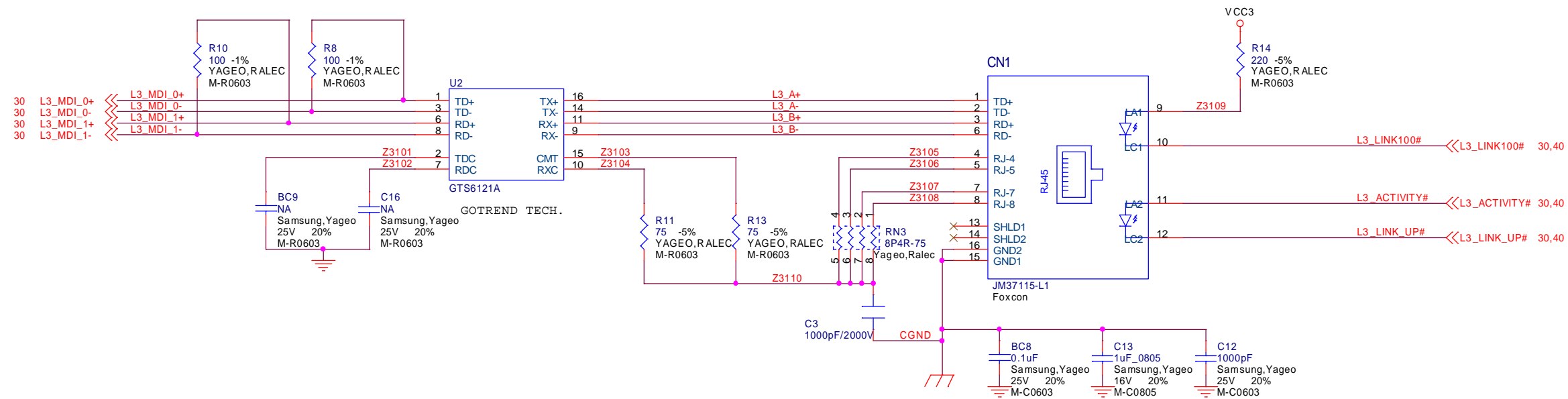


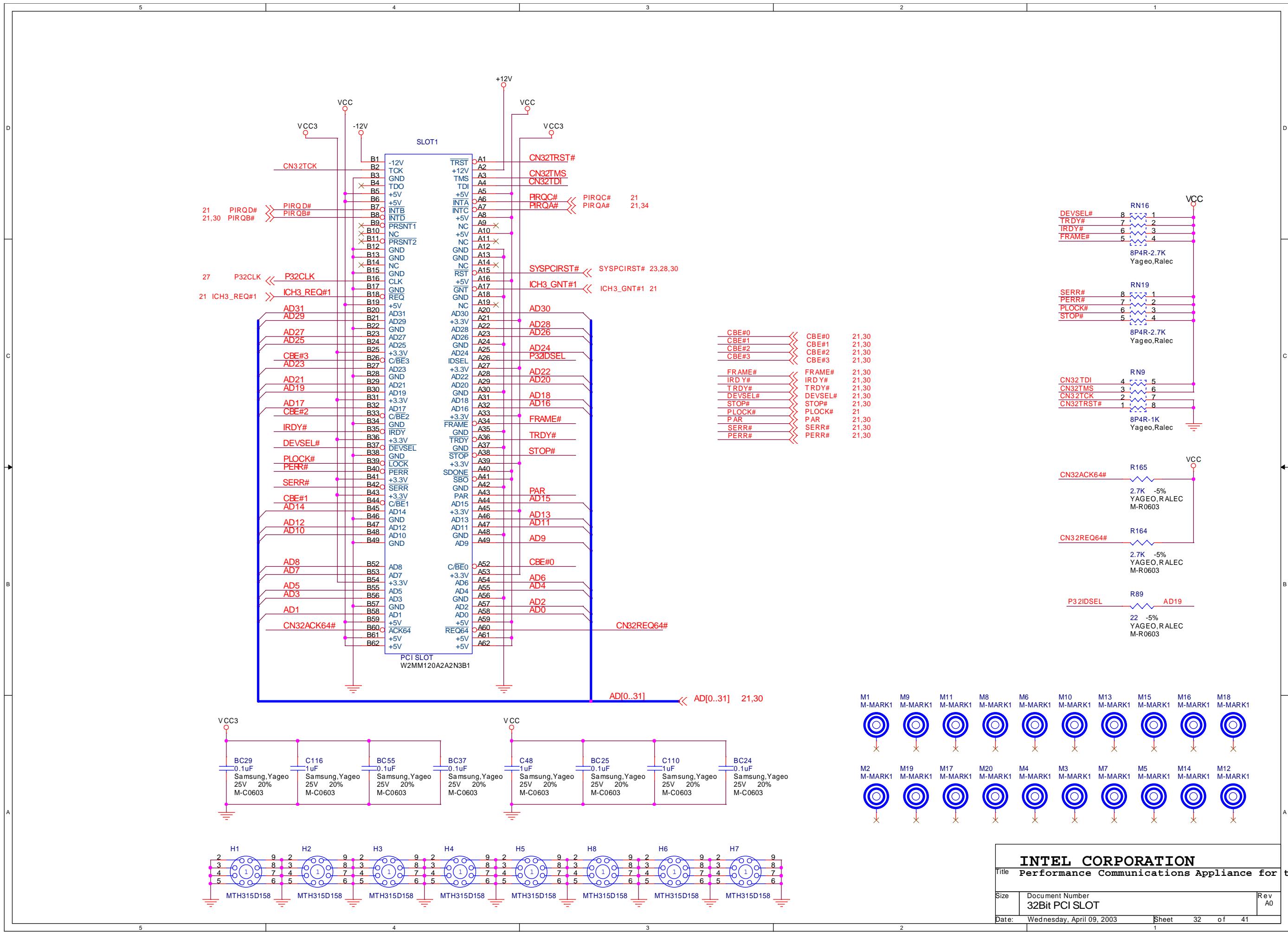




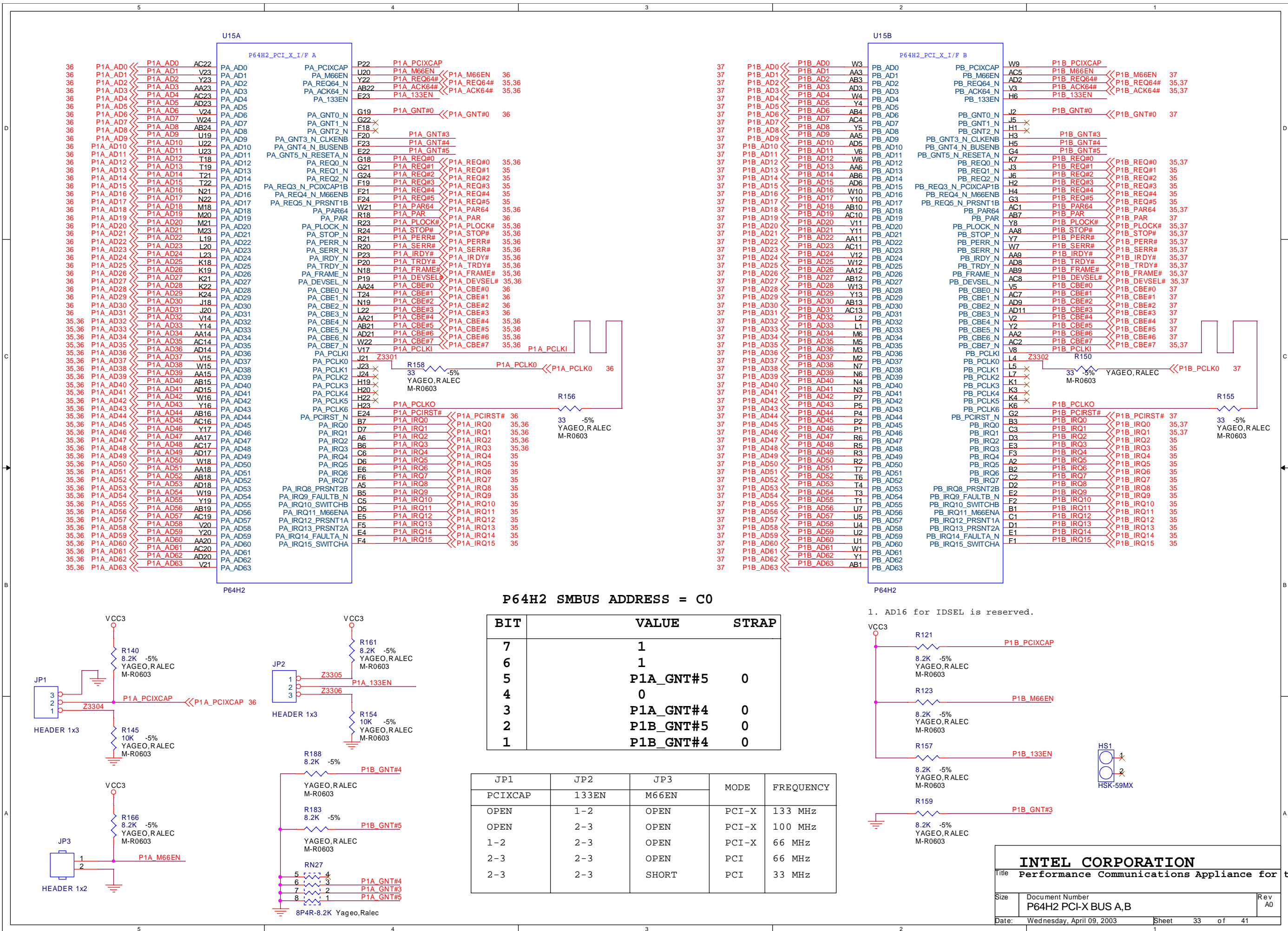










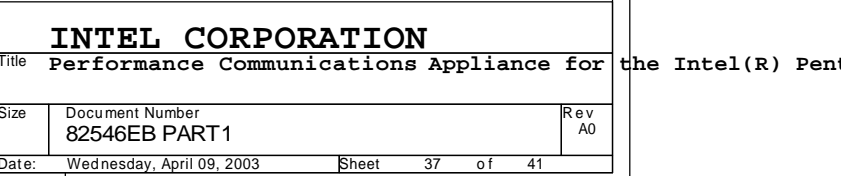












POWER REQUIREMENT:  
3.3V : 250mA  
2.5V : 500mA  
1.5V : 940mA

